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EEE412 High Gain Amplifier (HGA) Project

"I completed this project independently."

Introduction:

A High Gain Amplifier (HGA) is designed. The center frequency of the HGA is 390 MHz. A Class-A amplifier is designed for this process. For the BJT, BFU520W is used. The design specifications are listed below:

- Unconditionally stable at all frequencies (40MHz to 2GHz)
- Bandwidth: 10%
- Input return loss > 12dB in the band
- Output return loss > 12dB in the band
- Gain > 19 – 6.5×f (GHz) dB (f is the center frequency)
- Gain variation <± 0.5dB in the band

The lower band is 370.5 MHz, and the upper band is 409.5 MHz. Required gain of the circuit is calculated as 16.465 dB per the specification. Below table shows the requirements of this project.

Table 1: Design Requirements

LNA/HGA	f_0 (MHz)	$0.95f_0$ (MHz)	$1.05f_0$ (MHz)	Gain (dB)	Noise Figure (dB)	Input Return Loss (dB)	Output Return Loss (dB)
HGA	390 MHz	370.5 MHz	409.5 MHz	16.465 dB	Nothing specified	> 12dB	> 12dB

Fig. 1 shows the designed PCB. The bottom layer is completely allocated for ground. Because SMD capacitors are very sensitive, I tried not to use them as much as possible if the space permits.

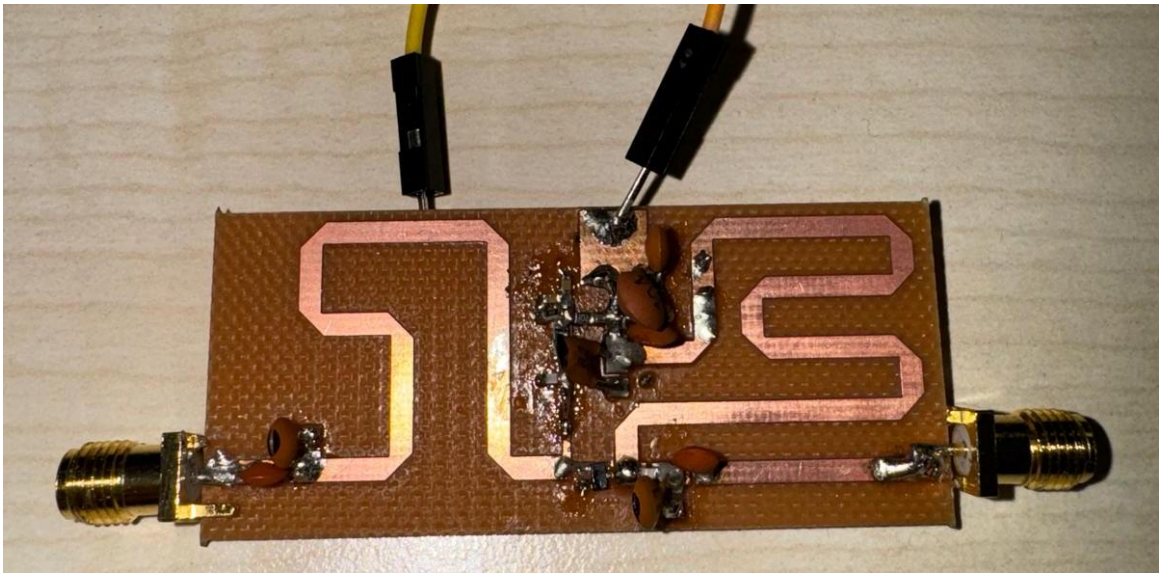

Fig. 1: Designed PCB

Analysis:

The designed HGA circuit on ADS with basic transmission lines is given in below figure.

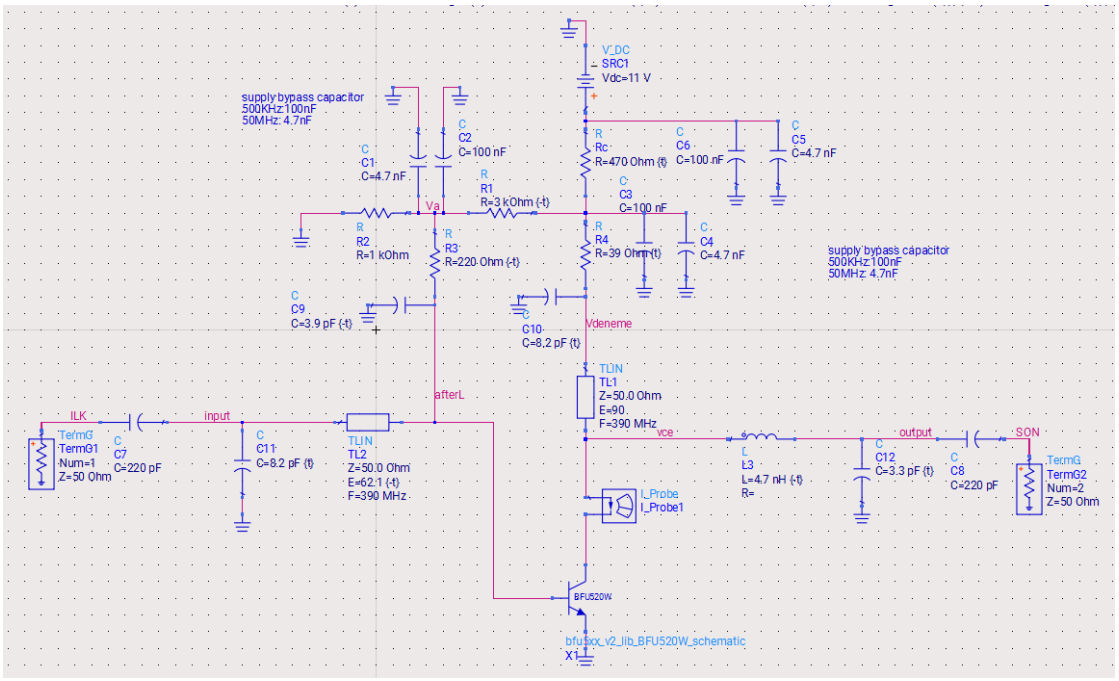

Fig. 2: Circuit schematic in ADS

After the part 2, I made some changes on the schematic in order to meet the design specifications after the soldering. Fig. 2 shows the final version of the circuit with the component values given. Below can be seen the biasing voltages of the circuit.

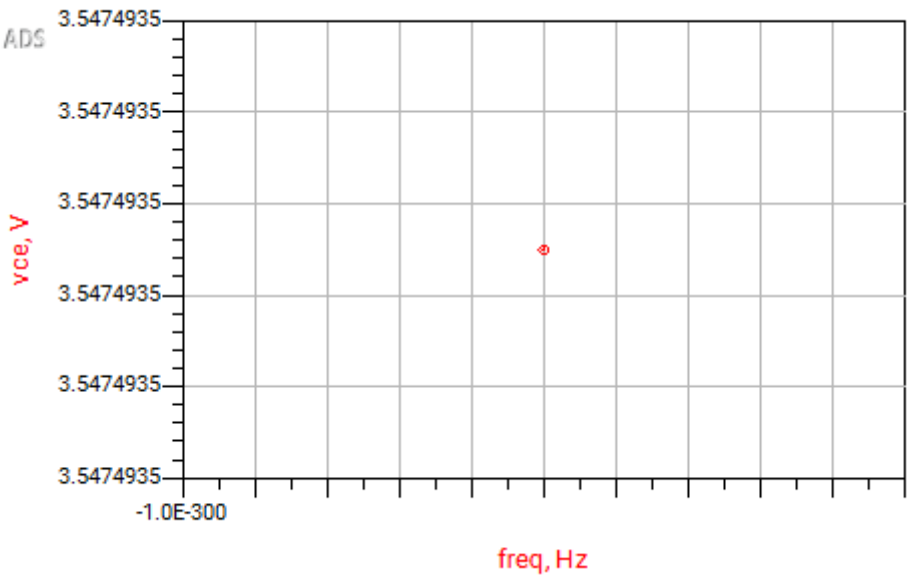

Fig. 3: Collector voltage measured in the simulation

In the previous part, the operating point of the circuit (collector voltage) is chosen as 5.08V. However, I changed the R1 resistor to 3KΩ in order to increase the gain of the circuit. Therefore, the collector voltage decreased to 3.54V. Fig. 4 shows the measured collector voltage, 3.375V, on the PCB.

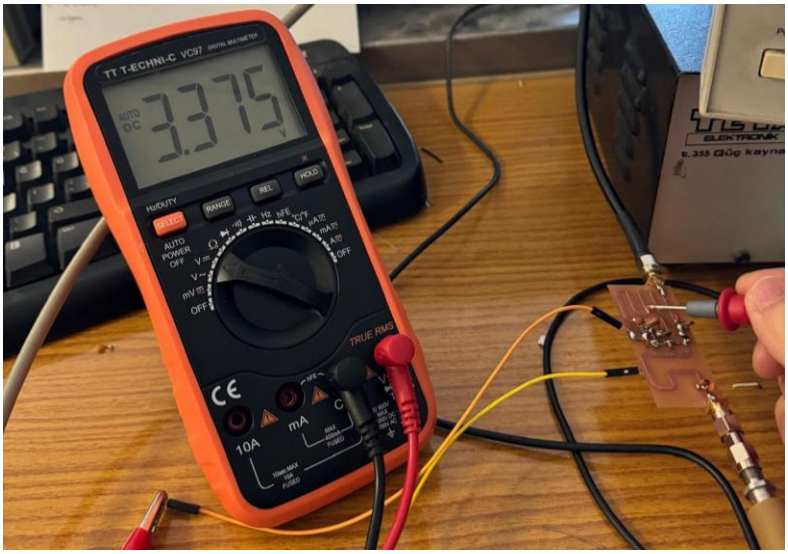

Fig. 4: Measured collector voltage of the transistor

In the simulation, base voltage of the transistor is measured as 897mV, as depicted in Fig. 5. Whereas in the hardware measurement, the base voltage is measured as 0.854mV, which can be seen in Fig. 6.

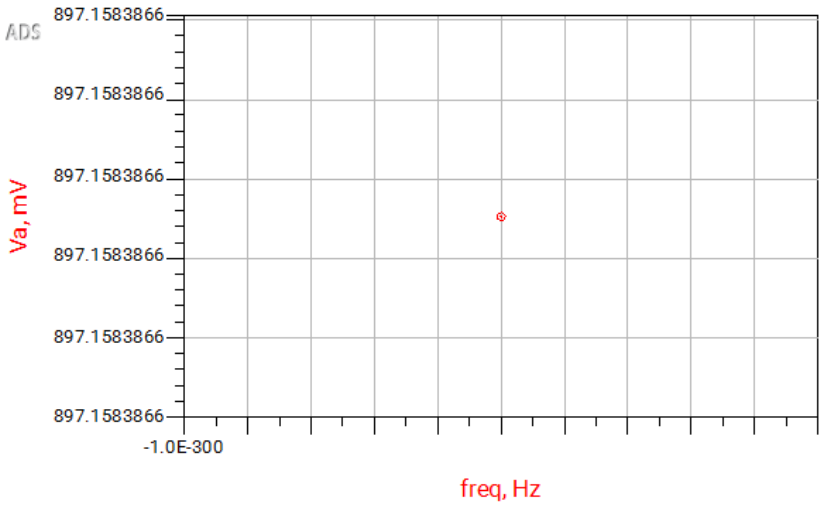

Fig. 5: Base voltage measured in the simulation

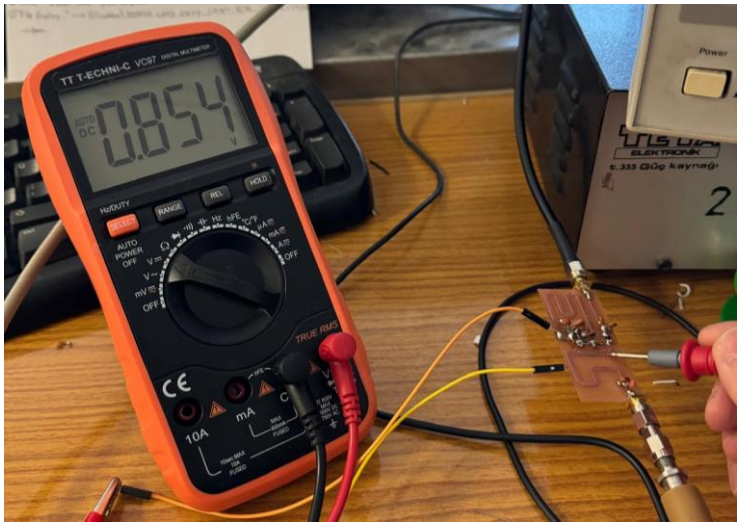

Fig. 6: Measured base voltage in hardware

Therefore, it can be said that the DC biasing of the circuit is successfully done. Next task is examining the S-parameters.

The S_{11} plot of the simulated circuit is given in Fig. 7.

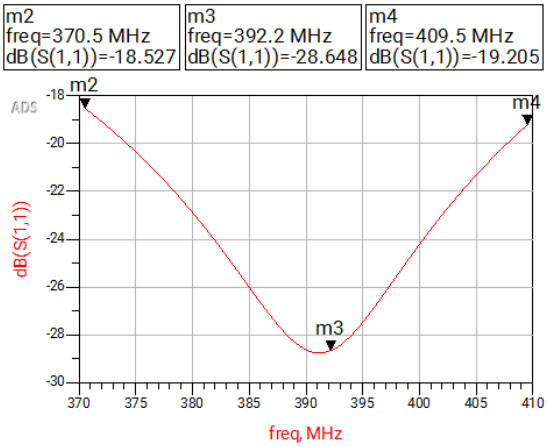

Fig. 7: S_{11} plot of the simulated circuit

The minimum S_{11} value is achieved around 390MHz, which is what is wanted. Also, inside the band, S_{11} values are lower than -12dB.

Fig. 8 shows the S_{22} of the simulated circuit.

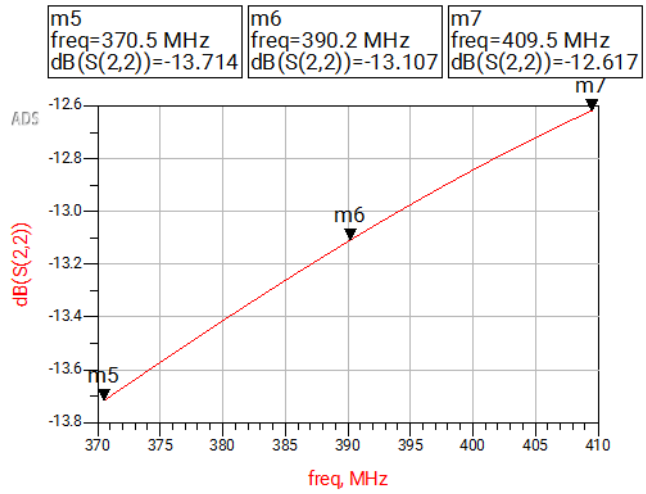

Fig. 8: S_{22} plot of the simulated circuit

As S_{11} plot, inside the band, the values for S_{22} are below -12dB.

Fig. 9 shows the S_{21} plot of the simulated circuit, which shows the gain of the circuit.

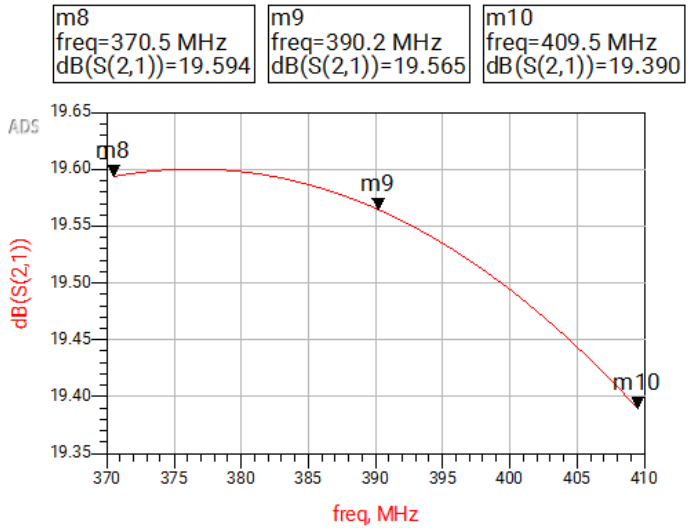

Fig. 9: S_{21} plot of the simulated circuit

As seen from Fig. 9, inside the band, the lowest gain achieved is 19.39dB. Fig. 10 shows the S-parameter plots of the hardware circuit. The top plot is for S_{11}, middle plot is for S_{21}, and bottom plot is for S_{22}.

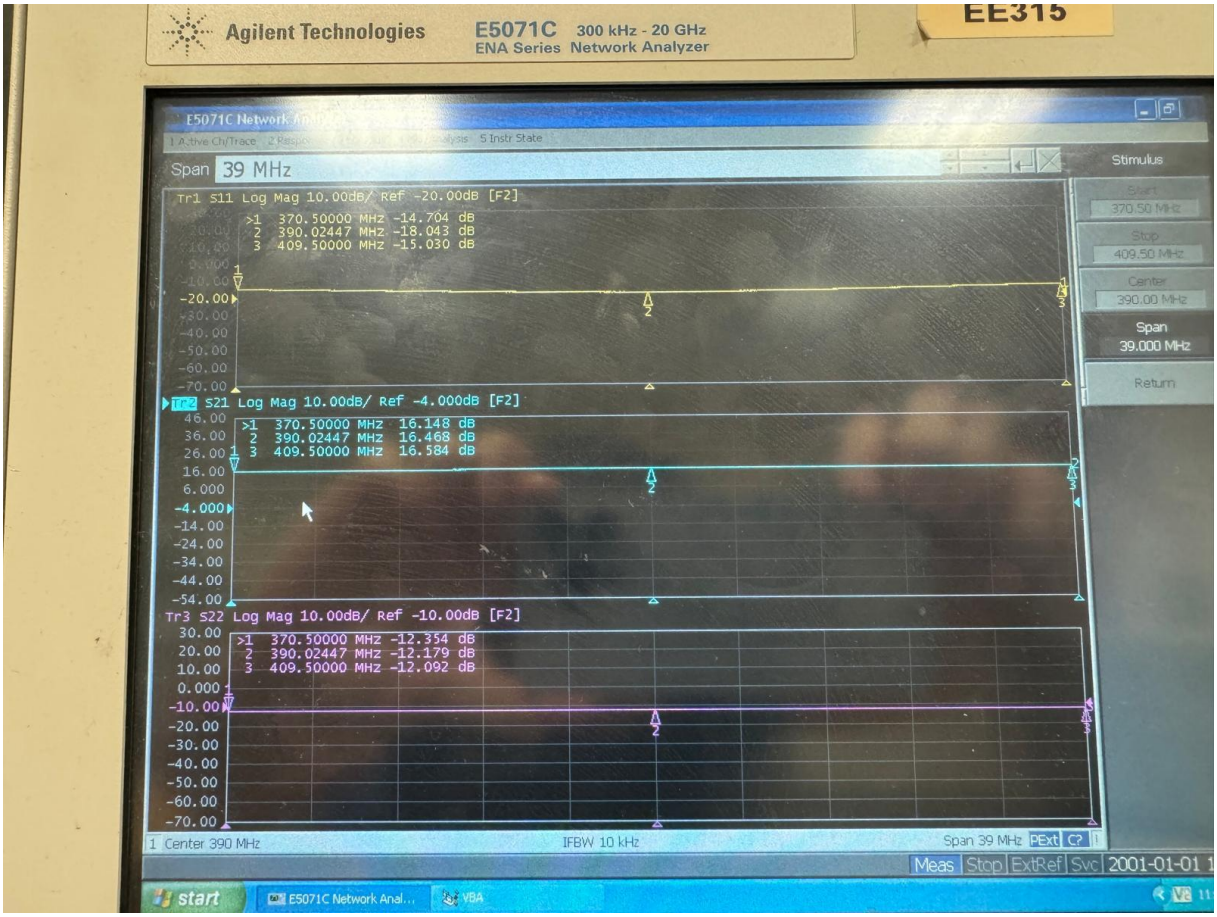

Fig. 10: S-parameters of the hardware circuit

Looking at the top plot, S_{11} plot, it is seen that inside the band, the maximum value is achieved at the lower band, 370.5 MHz, with a value of -14.704dB. In the middle plot, S_{21}, at the center frequency, gain is measured as 16.468dB. According to the design specifications, the gain must be greater than 16.465dB. Thus, the gain is right at the limit at the center frequency. Also, inside the band, the gain variation is measured as 0.436 dB, which is must be lower than 0.5 dB, as specified. Lastly, looking at the bottom plot, S_{22}, the maximum value is achieved at the upper band, 409.5 MHz, with a value of -12.092dB.

For the S_{11} and S_{22} plots, it is seen that inside the band, both have a value less than -12 dB, and for the S_{21} plot, at the center frequency, 390 MHz, the measured gain is 16.468dB. Therefore, all of the design specifications are successfully satisfied.

The worst input return loss value ($-|S_{11}|_{dB}$) inside the band is measured as 14.704dB at 370.5 MHz, and the worst output return loss value ($-|S_{22}|_{dB}$) inside the band is measured as 12.092dB at 409.5 MHz.

Lastly, noise figure of the hardware circuit was also measured. The noise figure of the designed HGA can be seen in Fig. 11.

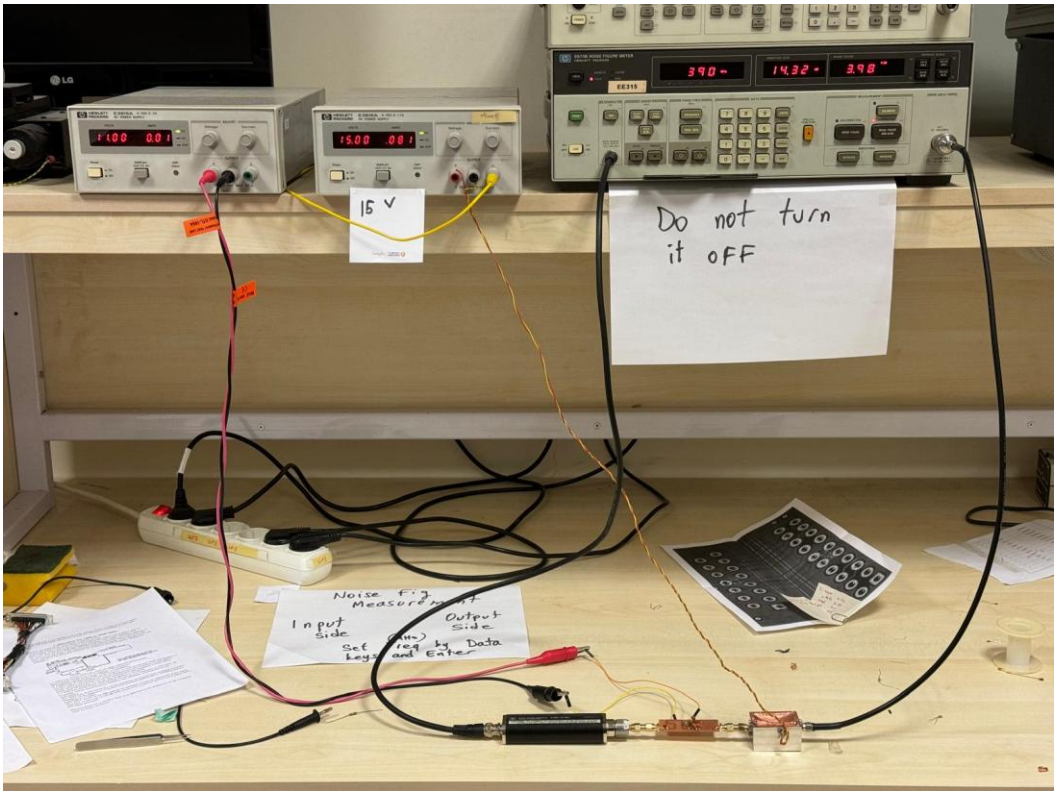

Fig. 11: Noise figure measurement setup

As seen from Fig. 11, the noise figure of the HGA is measured as 3.98dB at the center frequency, 390 MHz. At 370 MHz, noise figure is measured as 4.64dB, which can be seen from Fig. 12.

Fig. 12: Worst noise figure value measurement

In Fig. 13, you can see the measurement setup for the s-parameters with my circuit connected to it. The designed HGA is working with 11V supply voltage, and supply current is measured as 10mA.

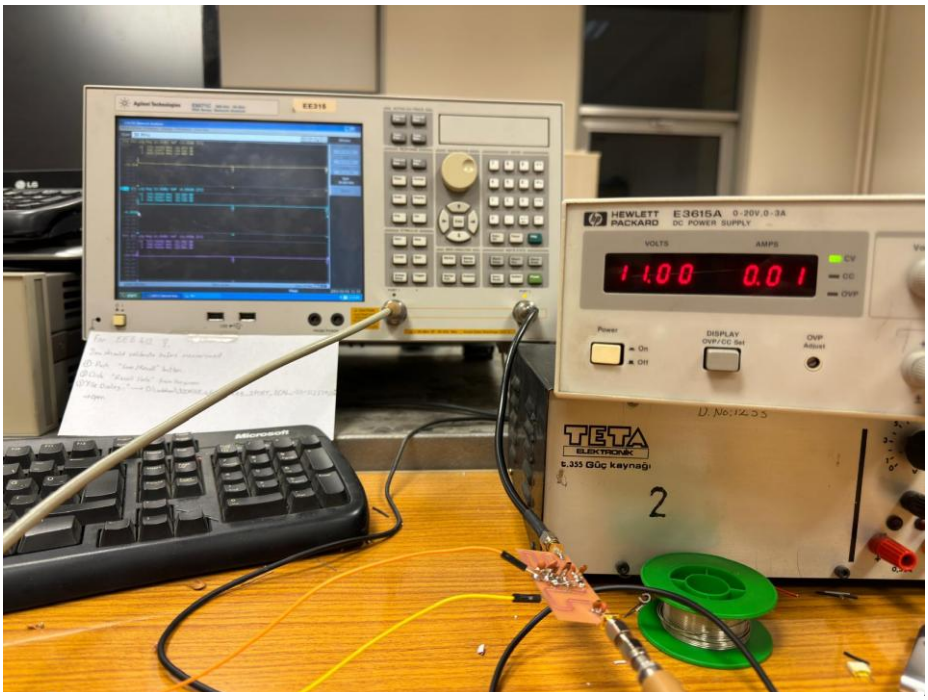

Fig. 13: S-parameter measuring setup

In the simulation, the supply current is measured as 15mA, which is shown in Fig. 14.

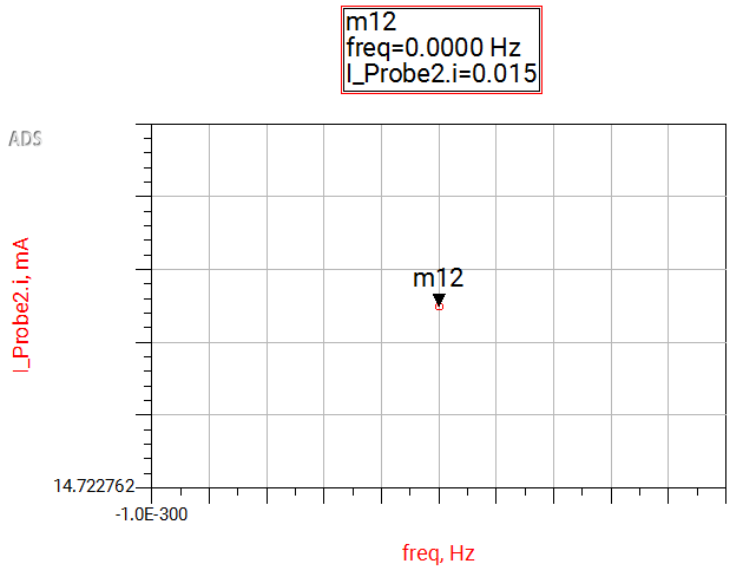

Fig. 14: Measured supply voltage in the simulation

Below table shows the measured values of the designed High Gain Amplifier circuit.

Table 2: Table of obtained values for HGA

Parameter	Measurement
Supply voltage (V)	11V
Supply current (mA)	10mA
Worst input return loss - S_{11} (dB)	14.709dB (370.5 MHz)
Worst output return loss - S_{22} (dB)	12.092dB (409.5 MHz)
Minimum S_{21} in the band (dB)	16.148dB (370.5 MHz)
Maximum S_{21} in the band (dB)	16.584dB (409.5 MHz)
Worst noise figure in the band (dB)	4.64dB (370.5 MHz)

From Table 2, it can be said that all of the design specifications are successfully achieved.

YouTube vide link: https://youtu.be/Ugf0bHKwn6k