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EEE412 “High Gain Amplifier” Project Report

Introduction

In this report, the design steps of a “High Gain Amplifier (HGA)” using a single BFU520W BJT will be shown. The center frequency of the HGA is assigned to be f = 0.39GHz. The design specifications are listed below:

- Source and load resistances are both 50Ω
- Unconditionally stable at all frequencies (40MHz to 2GHz)
- Bandwidth: 10%
- Input return loss > 12dB in the band
- Output return loss > 12dB in the band
- Gain > 19 – 6.5×f (GHz) dB (f is the center frequency)
- Gain variation <± 0.5dB in the band

Additionally, the PCB layout of the circuit schematic will be created with available components.

Methodology

The previously designed circuit schematic has a high-pass input matching network in the input side, therefore, it is changed to a low-pass topology. The new version of the circuit schematic is given in the figure below.

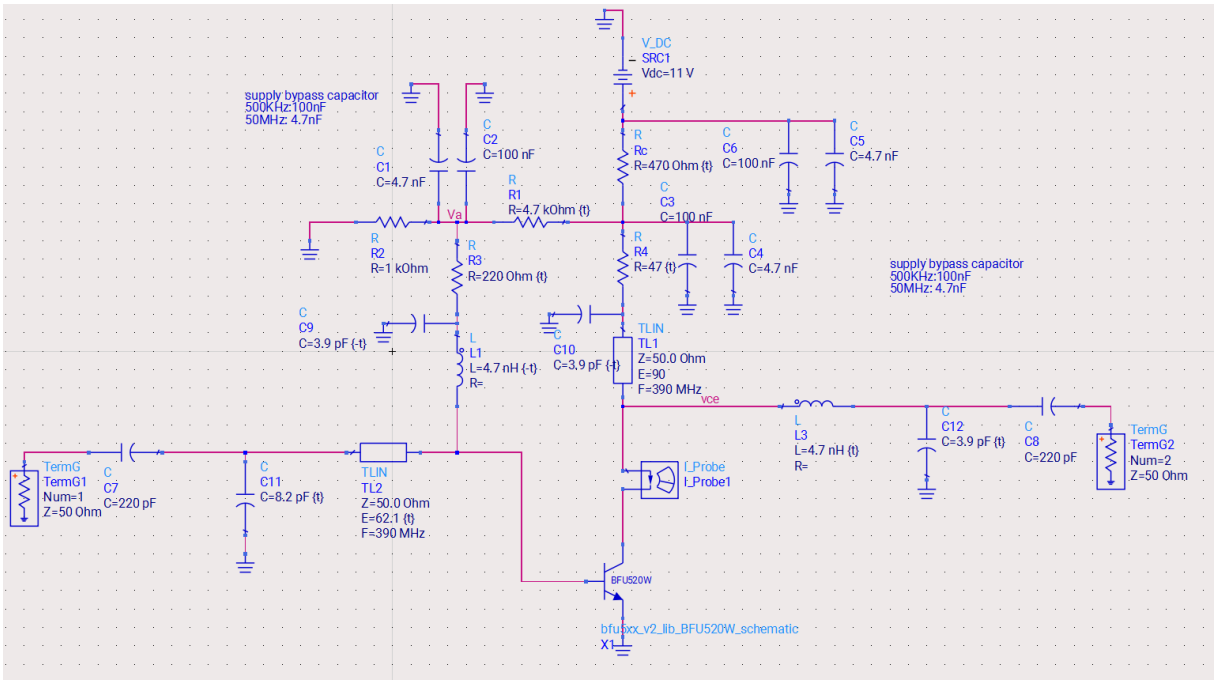


Fig. 1: Revised circuit schematic with available components used

Now, to be able to create a correct layout, lumped elements and transmission lines are changed so that their W and L values determined. Fig. 2 is the final value of the circuit schematic for the analysis purposes.

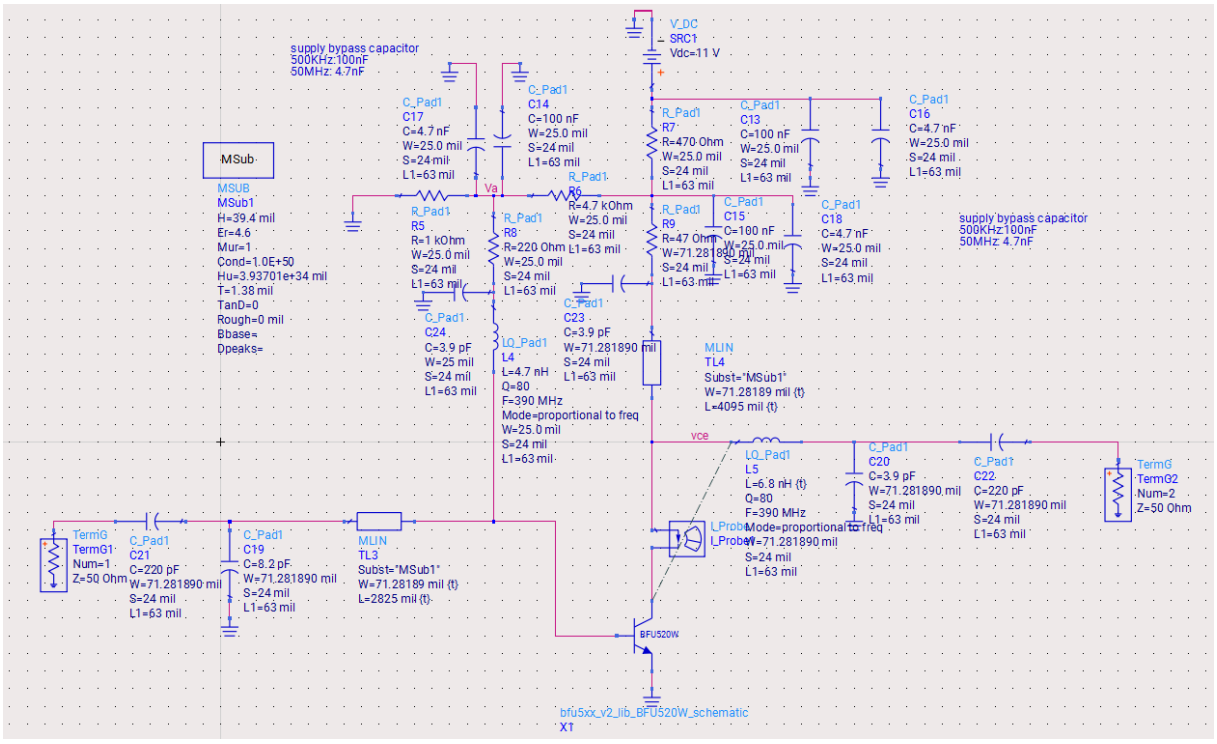


Fig. 2: Simulation circuit schematic

Analysis

Initially, the biasing of the circuit will be checked. The operation points of the transistor are chosen as V_{CE}=5V and I_C=10mA. Fig.3 shows the measured V_{CE} voltage from the schematic.

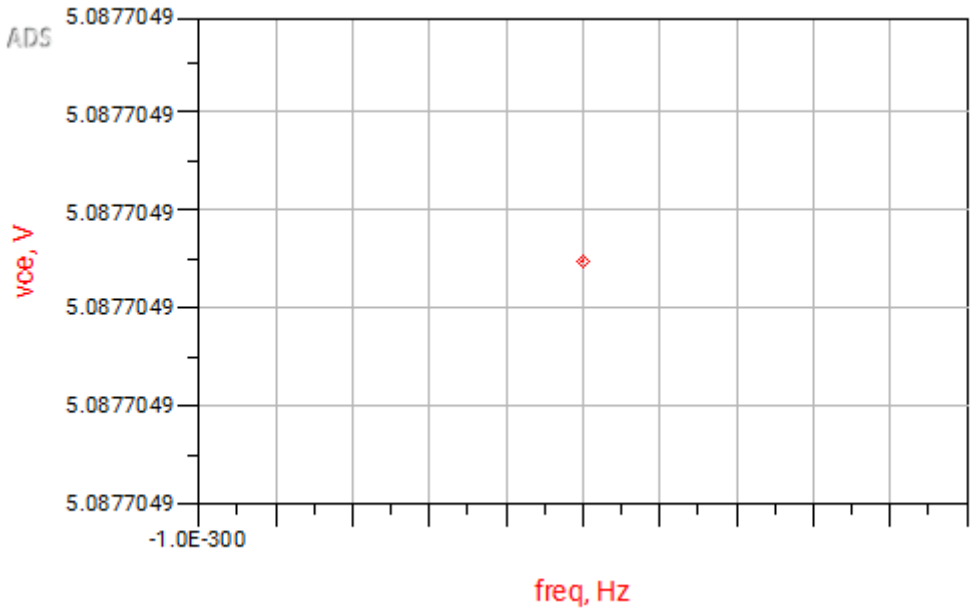


Fig. 3: V_{CE} voltage

Fig. 4 shows the collector current I_C of the transistor.

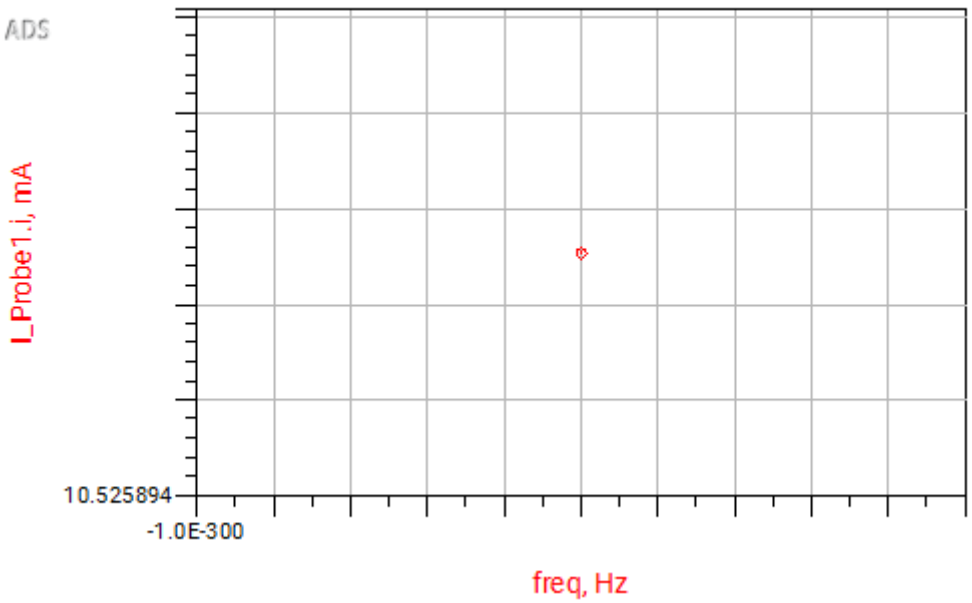


Fig. 4: I_C of the transistor

As mentioned, the chosen operating point is V_{CE} = 5V and I_C = 10mA. From Fig. 3 and Fig. 4, it can be seen that a V_{CE} of 5.08V is achieved and an I_C of 10.5mA current is achieved. The biasing of the circuit is done successfully. Additionally, the current going through R_2 resistor is set to $10I_B$, which is 1.053mA calculated earlier. Fig. 5 shows the measured voltage value at that node. R_2 value is chosen as 1KΩ.

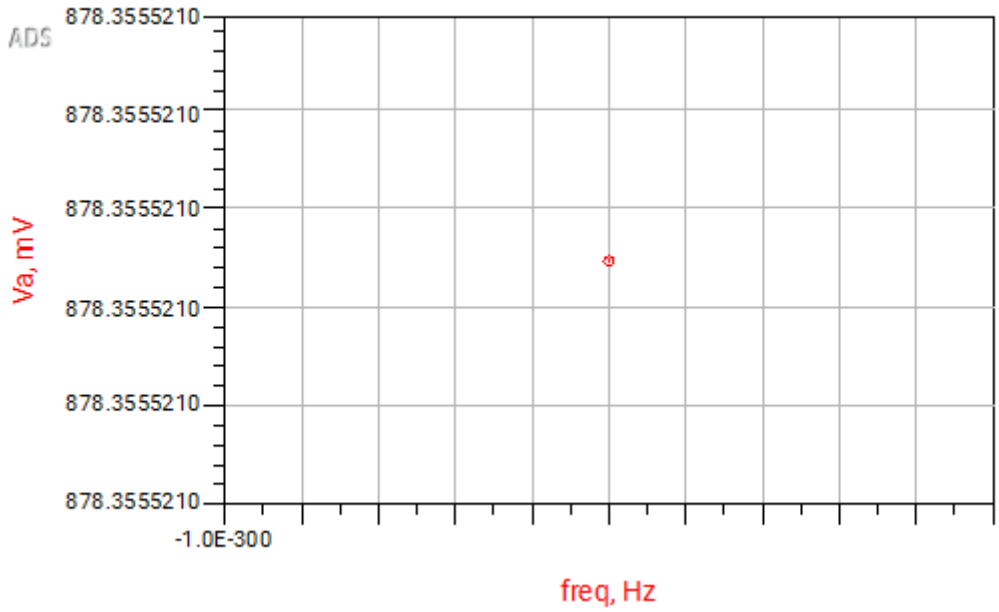


Fig. 5: Voltage at node A (V_0)

Using the Ohm's Law, the current going through R_2 resistor can be calculated.

$$V = IR$$

$$I = \frac{V}{R} = \frac{0.878}{1000} = 0.878mA$$

This value is calculated as 1.053mA initially, and at the simulation, a current value of 0.878mA is achieved. This concludes that the biasing network of the circuit is satisfactory.

To determine whether the circuit is stable, stability factor (K) of the circuit is plotted. If K>1, circuit is stable. Fig. 6 shows the stability factor plot of the circuit by indicating the minimum point.

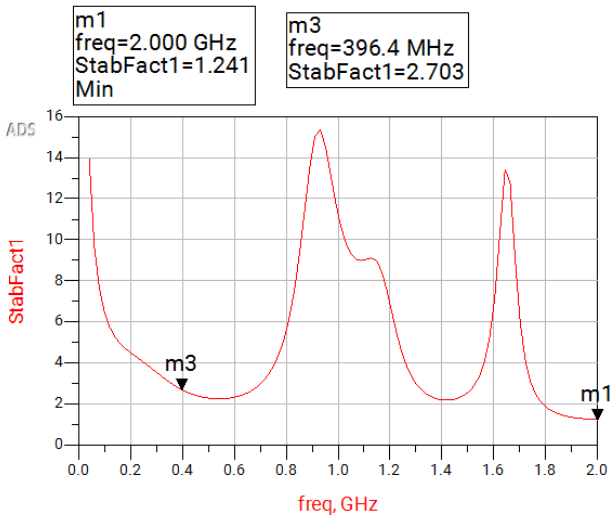


Fig. 6: Stability factor plot of the circuit

S_{11} and S_{22} plots of the circuit are given in the figures below respectively for the whole frequency range (40MHz – 2GHz).

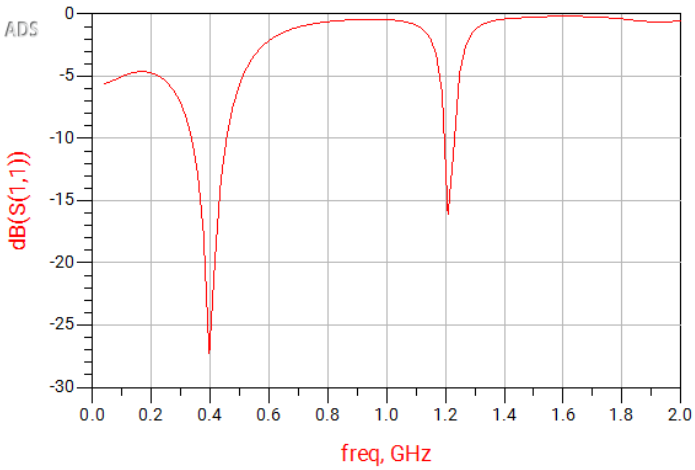


Fig. 7: S_{11} plot of the circuit

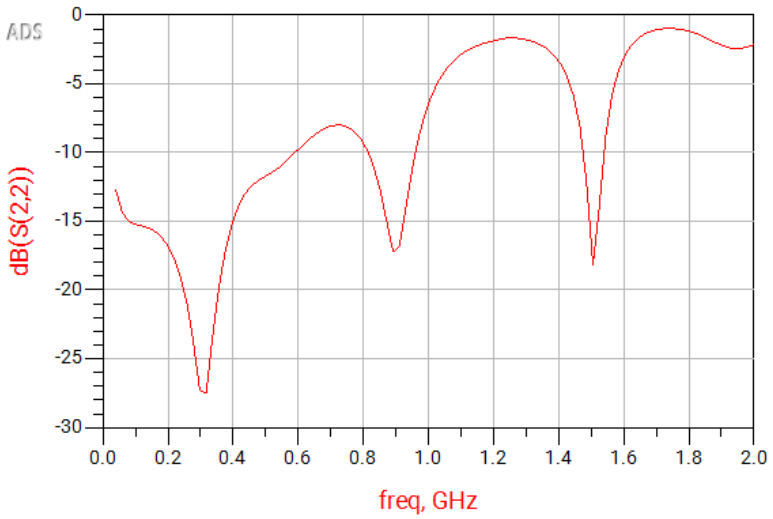


Fig. 8: S_{22} plot of the circuit

And for the 10% bandwith frequency range (370.5MHz – 409.5MHz), the S_{11} and S_{22} plots are given below respectively.

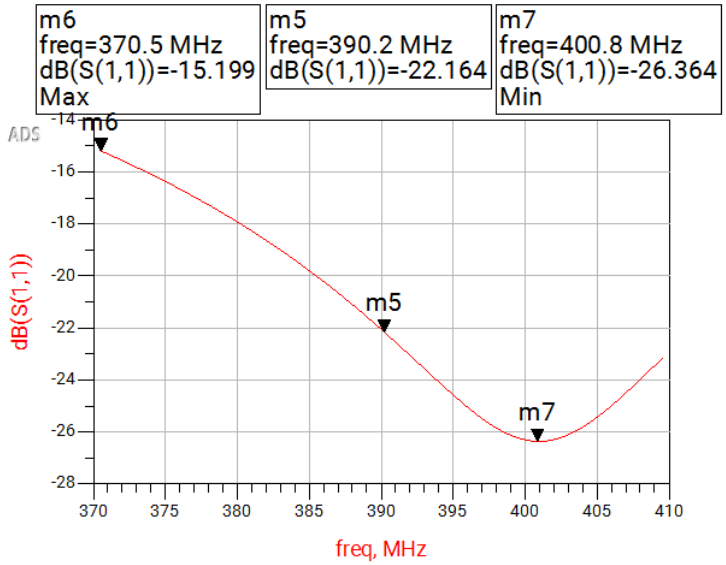


Fig. 9: S_{11} plot of the circuit inside the band

As seen from Fig. 9, at the center frequency 390MHz, S_{11} is measured as -22.164dB. Inside the band, the maximum value measured is -15.199dB, which is lower than the requirement -12dB. This requirement is also satisfied.

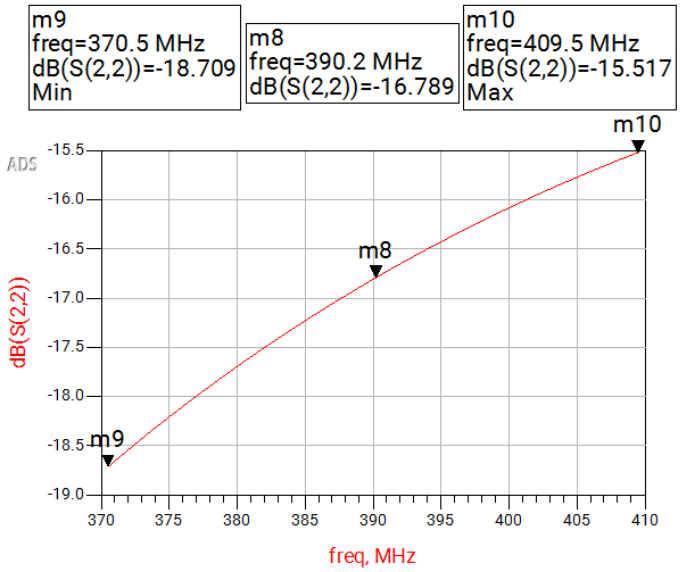


Fig. 10: S_{22} plot of the circuit inside the band

As seen from Fig. 10, at the center frequency 390MHz, S_{22} is measured as -16.789dB. Inside the band, the maximum value measured is -15.517dB, which is lower than the requirement -12dB. This requirement is also satisfied.

The S_{21} plot of the circuit is given in Fig. 11. The threshold gain is determined from the equation given in the Introduction. It was calculated as 16.465dB.

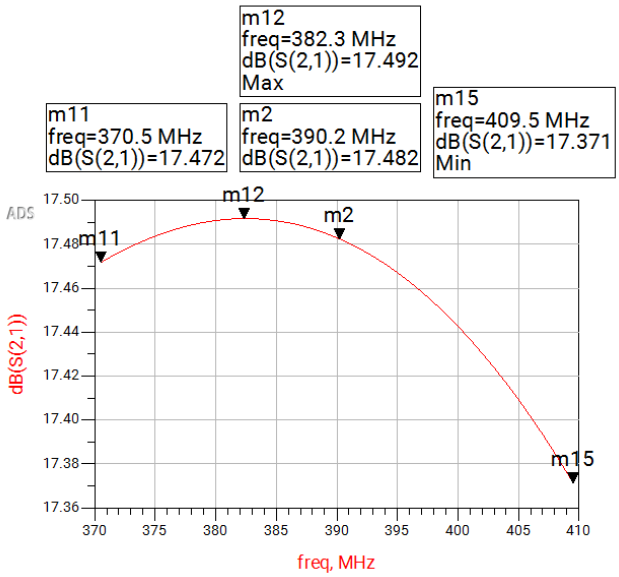


Fig. 11: S_{21} plot of the designed HGA

The minimum gain achieved inside the band is measured as 17.371dB, which is above the threshold value, 16.465dB. The gain requirement also satisfied. Moreover, the maximum gain achieved inside the band is measured as 17.492dB. The gain variation in the band is measured as 0.121dB, which is less than 0.5dB as specified in the design specifications. This requirement is also satisfied.

The noise figure of the circuit inside the band is shown in Fig. 12.

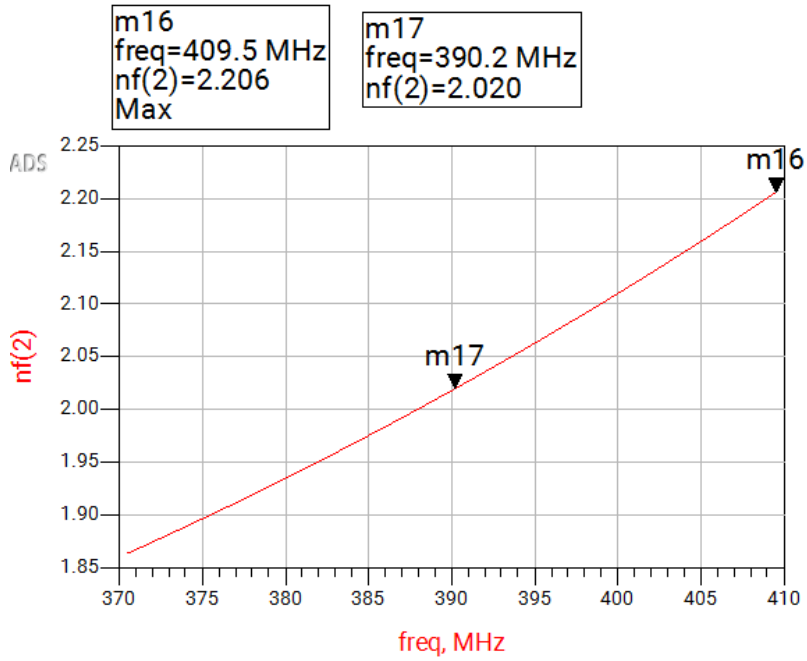


Fig. 12: Noise figure of the circuit inside the band

As seen from Fig. 12, at the center frequency, the measured noise figure of the HGA is 2.02, and inside the band, the highest noise figure value is measured as 2.206.

This concludes the analysis of the HGA with a full satisfaction of the design specifications.

The next task is to make necessary changes in the length of transmission lines so that they will fit inside the determine PCB dimensions.

PCB design

Firstly, I swapped the ground connections to VIAGND connections. For the emitter-ground connection, I used two parallel VIAGND's because each VIAGND acts like a small inductance, connecting them in parallel reduces the inductance by half, which reduces the effect on dB gain of the circuit. For each shunt capacitor, I used one VIAGND per shunt capacitor. Total number of VIAGNDs used in the schematic is 14 in total. Furthermore, VIAGND's changed the S_{11}, S_{22}, and Gain of the circuit. Therefore, an additional tuning performed on the schematic to get the desired results again.

At the both end of the matching networks, a 50Ω transmission line is inserted until reaching the side of the PCB. These are for the SMA connector. For the specified values, at 390MHz, a 50Ω transmission line has a measured width(W) of 71.28189mils.

To fit the design into 2300x1000 mils board, I changed the length of the used transmission lines in the circuit, and bended them to use the area effectively. In Fig. 2, TL3 has a total length of 2825mils. With tuning, the new length of that transmission line determined as 2250mils. Again from Fig. 2, TL4 has a total length of 4095mils. With tuning, the new length of that transmission line determined as

3059mils. Fig. 13 shows the source and load unit stability circles and Fig. 14 shows the plot for stability factor (K) from 40MHz to 2GHz.

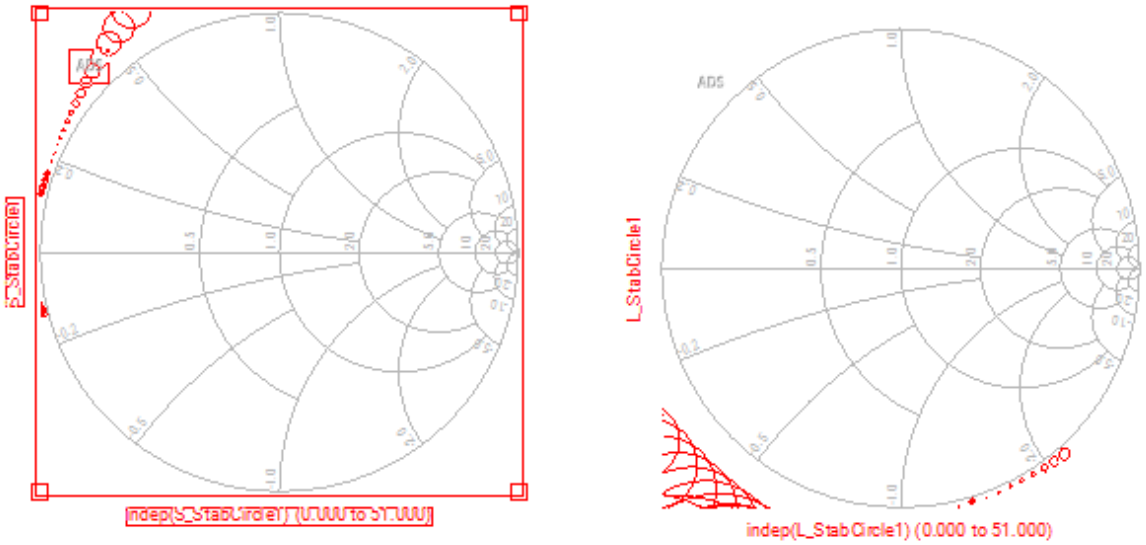


Fig. 13: Source and load unit stability circles

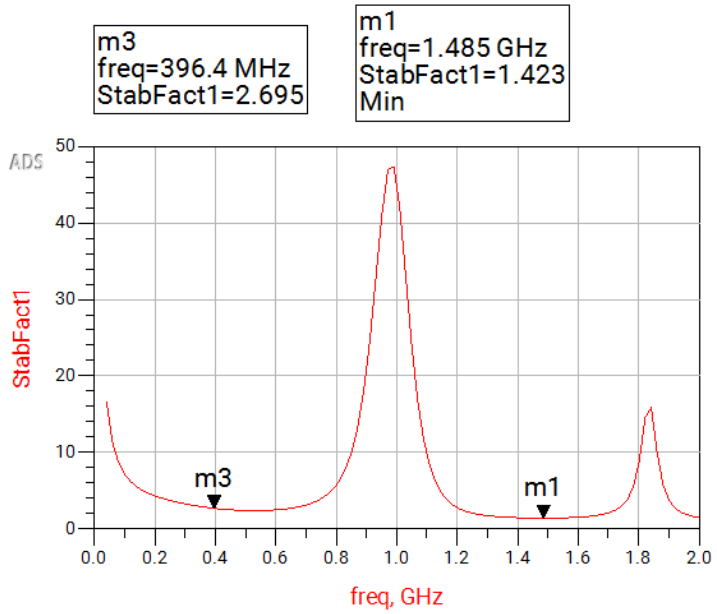


Fig. 14: Stability factor (K) plot

As seen from Fig. 13, the stability circles are outside the unity Smith chart, and looking at Fig. 14, stability factor (K) value is always above 1. Those results show that circuit is unconditionally stable at all frequencies from 40MHz to 2GHz.

The S_{11} and S_{22} plots in dB inside the 10% bandwith are given in below figures respectively.

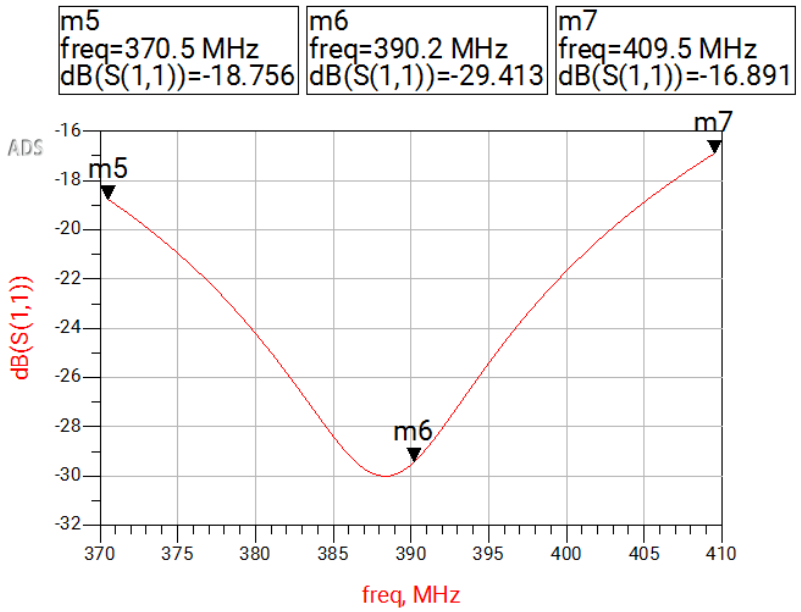


Fig. 15: S_{11} plot of the final schematic

As seen from the above figure, inside the band, the maximum value is measured as -16.891, which is less than -12dB, as specified in the design specifications.

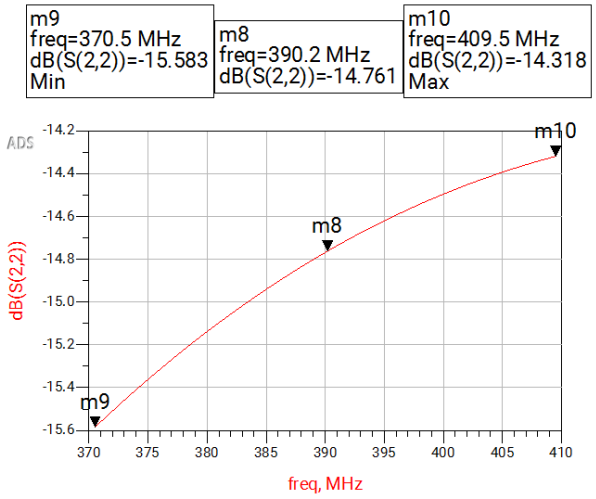


Fig. 16: S_{22} plot of the final schematic

As seen from the above figure, inside the band, the maximum value is measured as -14.318, which is less than -12dB, as specified in the design specifications.

The dB gain of the circuit is given in Fig. 17.

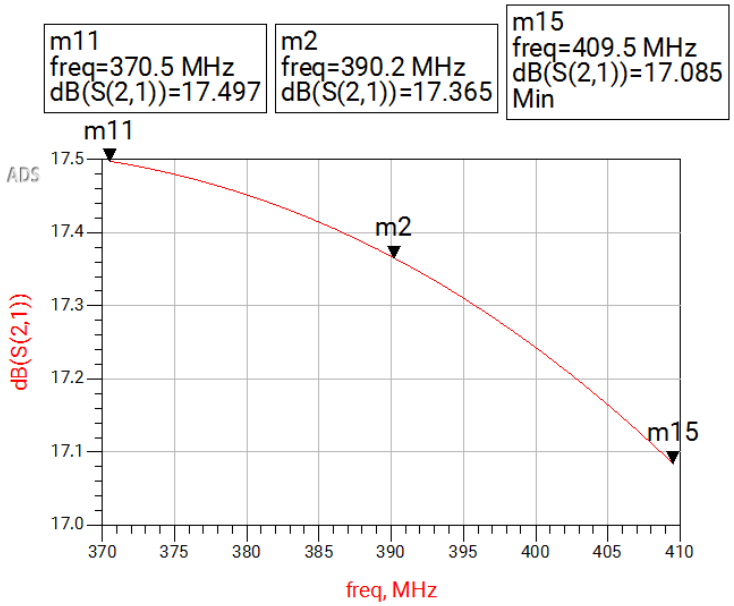


Fig. 17: Gain of the final version of the circuit

Inside the band, the maximum gain is measured as 17.497dB and minimum gain is measured as 17.365dB. The gain variation inside the band is calculated as 0.412dB, which is less than 0.5dB. Additionally, at the center frequency, the dB gain is measured as 17.365dB.

Finally, the noise figure of the circuit inside the band is depicted in the below figure.

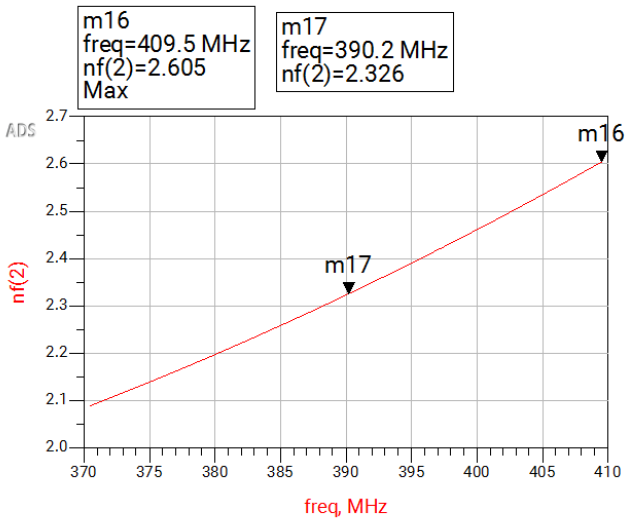
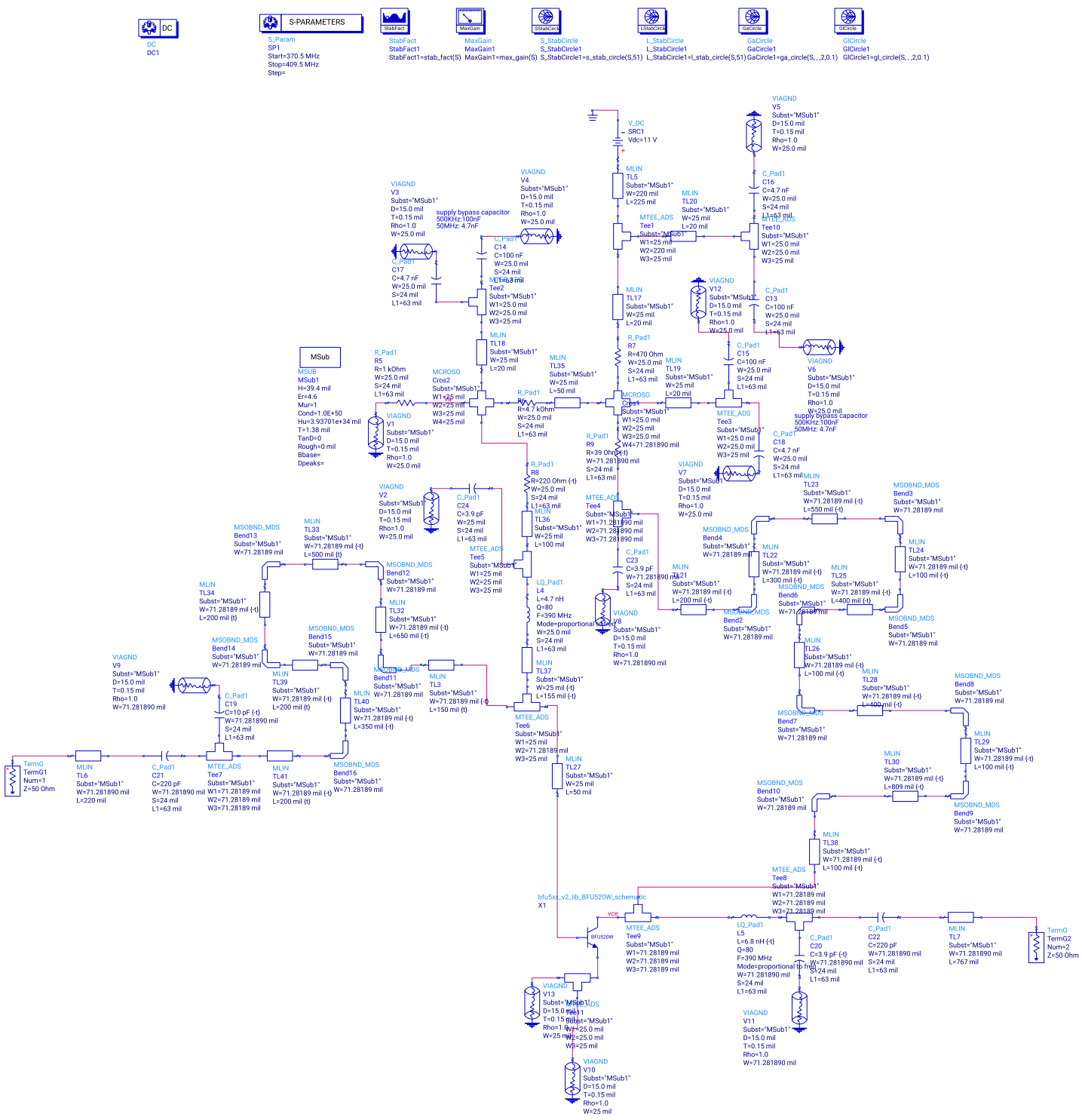


Fig. 18: Noise figure of the final version of the circuit

The highest noise figure inside the band is measured at 409.5MHz with a value of 2.605.

The schematic of the circuit is given in the following page.


DC
DC
DC1
S-PARAMETERS
S_Param
SP1
Start=370.5 MHz
Stop=409.5 MHz
Step=
StabFact
StabFact1
StabFact1=stab_fact(S)
MaxGain
MaxGain1
MaxGain1=max_gain(S)
S_StabCircle
S_StabCircle1
S_StabCircle1=s_stab_circle(S,51)
L_StabCircle
L_StabCircle1
L_StabCircle1=l_stab_circle(S,51)
GaCircle
GaCircle1
GaCircle1=ga_circle(S, , ,2,0.1)
GlCircle
GlCircle1
GlCircle1=gl_circle(S, , ,2,0.1)
MSub
MSUB
MSub1
H=39.4 mil
Er=4.6
Mur=1
Cond=1.0E+50
Hu=3.93701e+34 mil
T=1.38 mil
TanD=0
Rough=0 mil
Bbase=
Dpeaks=
V_DC
SRC1
Vdc=11 V
bfu5xx_v2_lib_BFU520W_schematic
X1
BFU520W
TermG
Term01
Num=1
Z=50 Ohm
TermG
TermG2
Num=2
Z=50 Ohm
supply bypass capacitor
500KHz:100nF
50MHz: 4.7nF

The board outline is specified as 2300x1000mils. Converting to mm, it is 58.4x25.4 mm. Fig. 19 shows the ruler depicting the sides of the board.

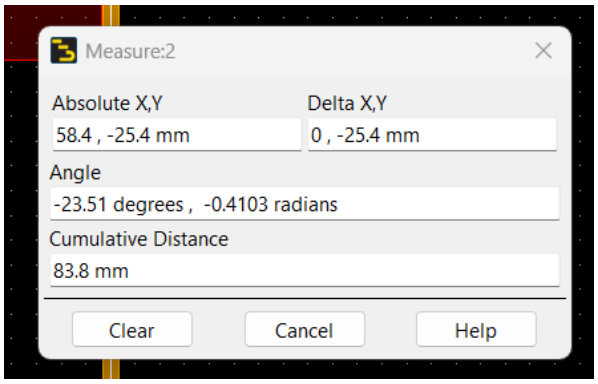


Fig. 19: Board outline measurements

The top layer image of the designed PCB is given in Fig. 20.

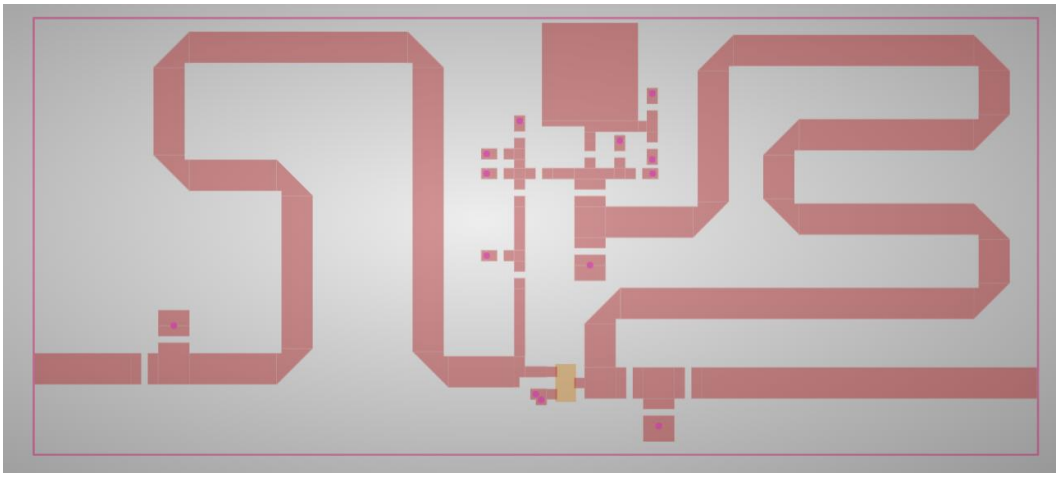


Fig. 20: Top layer of the designed PCB

The drill locations are also given in the following figure.

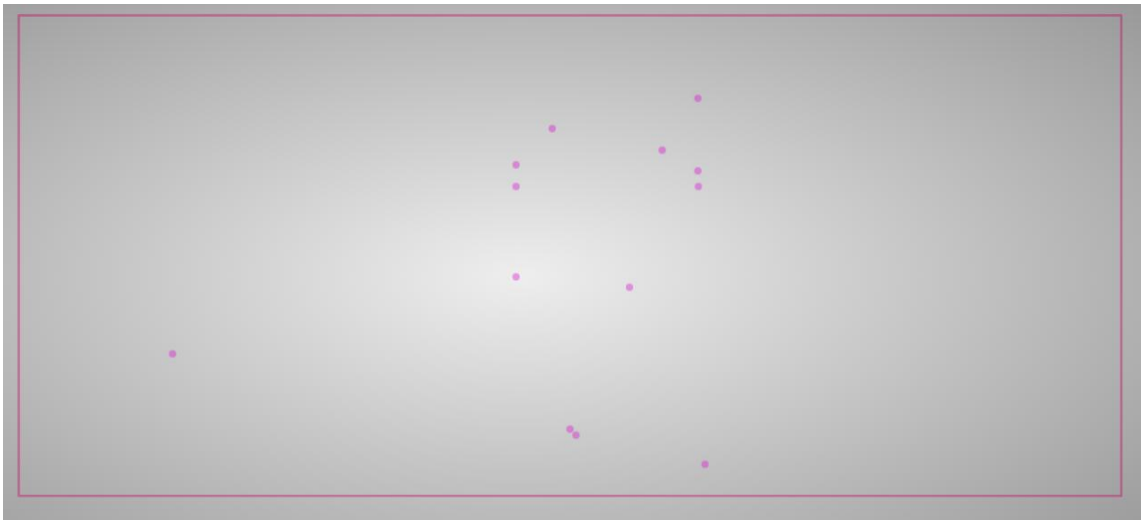
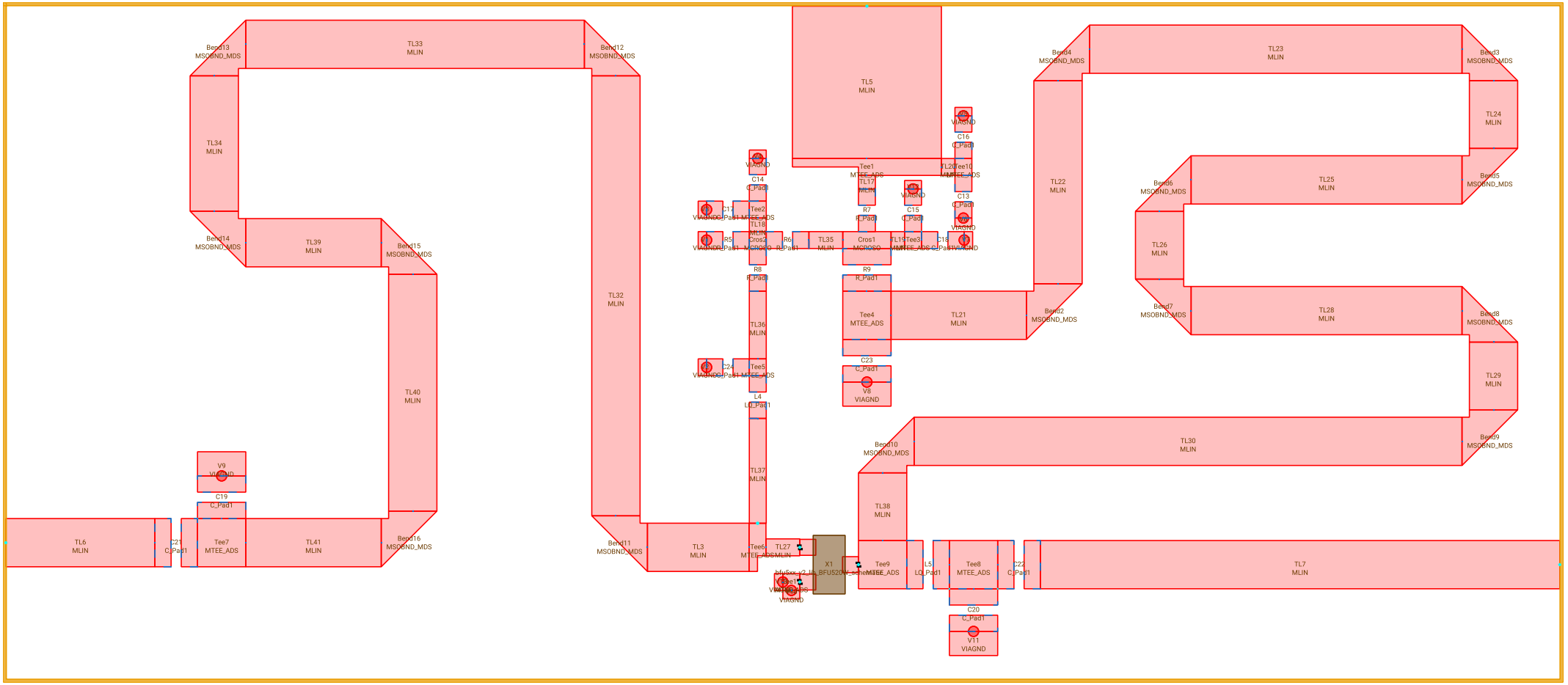


Fig. 21: Drill locations of the designed PCB

In the following page, the designed layout of the circuit can be seen. As mentioned, for the SMA connectors, a transmission line of 50Ω is added and extended to the sides of the board.


Bend13
MSOBND_MDS
TL33
MLIN
Bend12
MSOBND_MDS
TL34
MLIN
TL5
MLIN
Bend4
MSOBND_MDS
TL23
MLIN
Bend3
MSOBND_MDS
TL24
MLIN
TL22
MLIN
Bend6
MSOBND_MDS
TL25
MLIN
Bend5
MSOBND_MDS
TL26
MLIN
Bend14
MSOBND_MDS
TL39
MLIN
Bend15
MSOBND_MDS
TL32
MLIN
TL40
MLIN
TL36
MLIN
Tee4
MTEE_ADS
TL21
MLIN
Bend2
MSOBND_MDS
Bend7
MSOBND_MDS
TL28
MLIN
Bend8
MSOBND_MDS
TL29
MLIN
TL37
MLIN
Bend10
MSOBND_MDS
TL30
MLIN
Bend9
MSOBND_MDS
TL38
MLIN
TL6
MLIN
Tee7
MTEE_ADS
TL41
MLIN
Bend16
MSOBND_MDS
Bend11
MSOBND_MDS
TL3
MLIN
Tee6
MTEE_ADS
TL27
MLIN
X1
Tee9
MTEE_ADS
Tee8
MTEE_ADS
TL7
MLIN
VIAGND
C_Pad1
R_Pad1
L_Pad1
LQ_Pad1
Tee1
MTEE_ADS
Tee2
MTEE_ADS
Tee3
MTEE_ADS
Tee5
MTEE_ADS
Cros1
MCROSO
Cros2
MCROSO
TL17
MLIN
TL18
MLIN
TL19
MLIN
TL35
MLIN
TL2
MLIN
L4
L5
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
R5
R6
R7
R8
R9
V8
V9
V11