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EEE415 Final Schematic Report

Introduction: An integrated circuit OPAMP is designed with the given specifications. The specifications are listed below:

- Output voltage voltage noise, tested as described below, <60 nV/√Hz @10kHz
- Gain bandwidth product (unity gain bandwidth) >10MHz
- Voltage supply 1.8V
- Should be able to drive at least 5pF capacitance
- Output voltage swing, 0.4V-1.4V
- Open loop DC gain >100dB with 5kΩ connected to the output
- Power: minimize <1mA is possible
- You are given a reference current of 10µA, and generate the required biasing, no additional supplies except 1.8V

Methodology: For the design, a nested miller compensation based OPAMP topology is used. This topology includes 3 stages. First stage is created by a 5 transistor OTA circuit followed by a PMOS common source stage. The last stage is a NMOS common source stage. In order to stabilize the circuit, two capacitors are used. The purpose of these capacitors is generating poles. Because the gain of the circuit is high, stability of the circuit is provided by the additionally generated poles.

The gain of the nested miller compensation based OPAMP is high compared to two-stage OPAMP designs. The reason for choosing this topology is because I cannot make the output buffer stage work. Therefore I think generating a high enough gain will provide a gain higher than 100dB while the circuit drives 5KΩ load.

The total noise contributor of the circuit is the 5 transistor OTA circuit. In order to reduce the noise, W*L product is taken into consideration due to 1/f noise and thermal noise formulas and therefore g_m formula. Fig. 1 shows the designed circuit schematic.

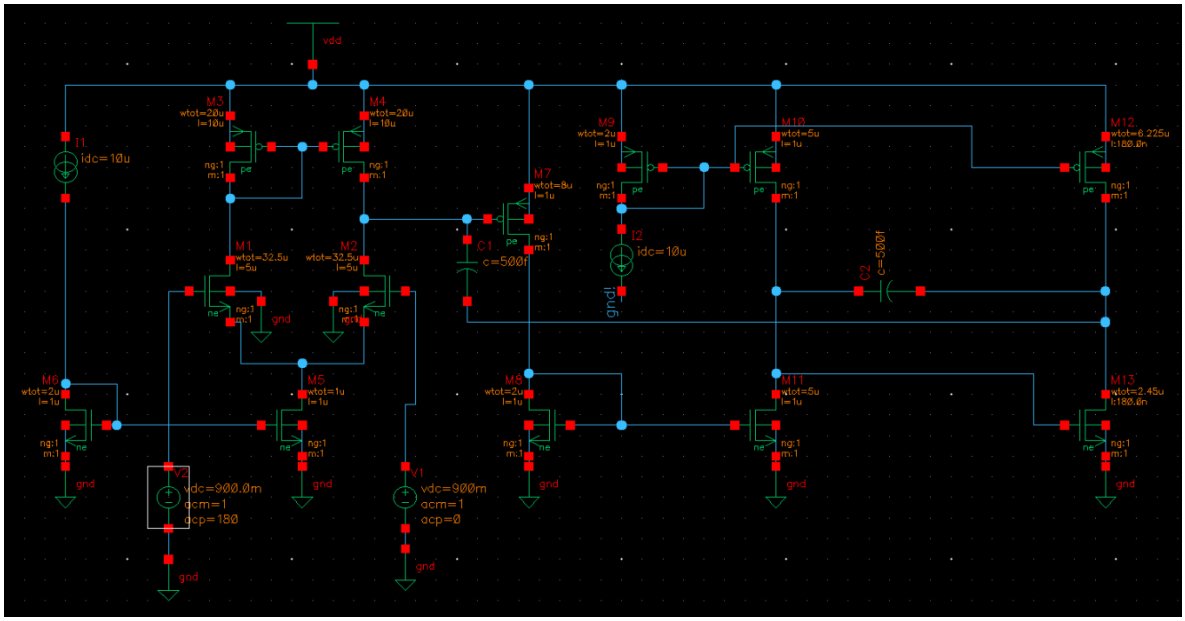

Fig. 1: Designed circuit schematic

The design values of the used MOS devices in the OPAMP is given in the table below:

Component	W(Width) in µm	L(Length) in µm
M1	32.5	5
M2	32.5	5
M3	20	10
M4	20	10
M5	1	1
M6	2	1
M7	8	1
M8	2	1
M9	2	1
M10	5	1
M11	5	1
M12	6.225	0.18
M13	2.45	0.18

The design values of the used capacitors in the OPAMP is given in the table below:

Component	Farad
C1	500f
C2	500f

As stated, because the gain of the circuit is large and in order to meet both the unity-gain bandwith and phase margin specifications, we need additional poles. C1 and C2 capacitors are generating additional poles. As seen from Fig. 1, the gain curve in the bode plot starts directly by decreasing, this is because the initial pole, caused by C1. The other pole is chosen as far apart enough so that the phase of the circuit do not decreases rapidly, the second capacitor value C2 is chosen regarding this issue.

Analysis: The gain of the circuit when driving 5pF capacitor and load resistance is not connected is measured as 138dB at 1Hz. Unity gain bandwith of the circuit is measured as 20.98MHz, unity gain of the OPAMP is the point where the dB gain is 0dB. For the phase margin, first the frequency at 0dB is found, which is measured as 20.98 MHz. At this frequency, phase of the OPAMP is measured as -131.21 degrees. The phase margin of the circuit is calculated from the following formula: ϕ – (-180). The corresponding phase margin is (-131.21) – (-180) = 48.79 degrees, which meets the specification. For the gain margin, the dB gain at -180 degree is measured, and found as -1.87 dB. Because dB gain is less than zero, this system is stable.

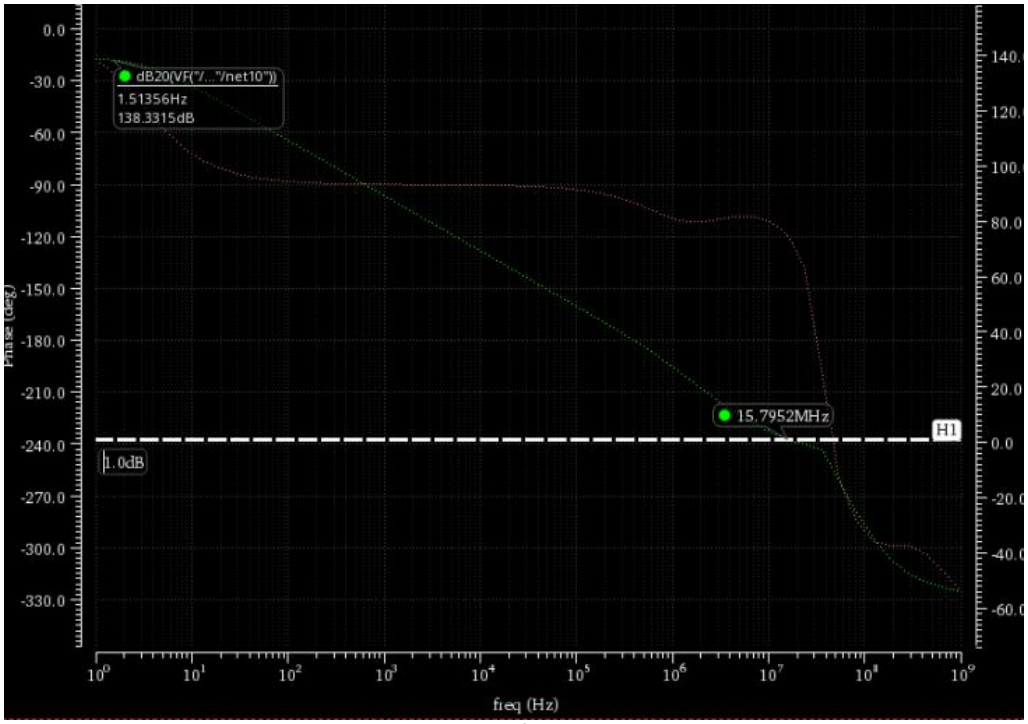

Fig. 2: Gain of the OPAMP

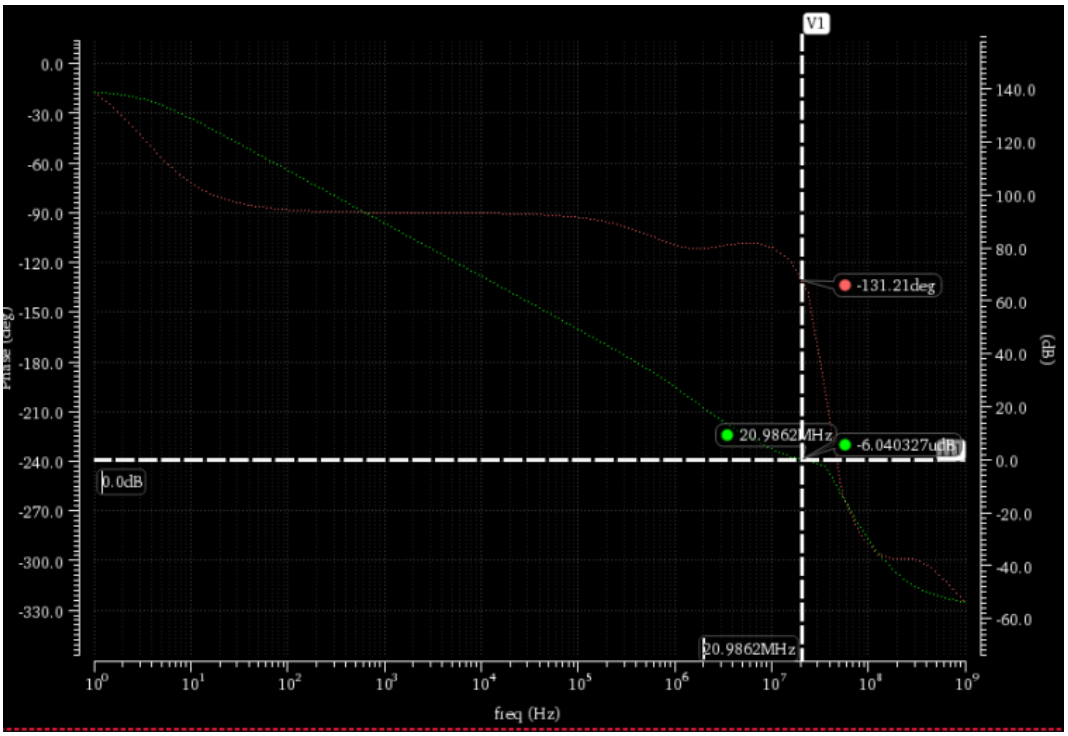

Fig. 3: Phase margin of the OPAMP

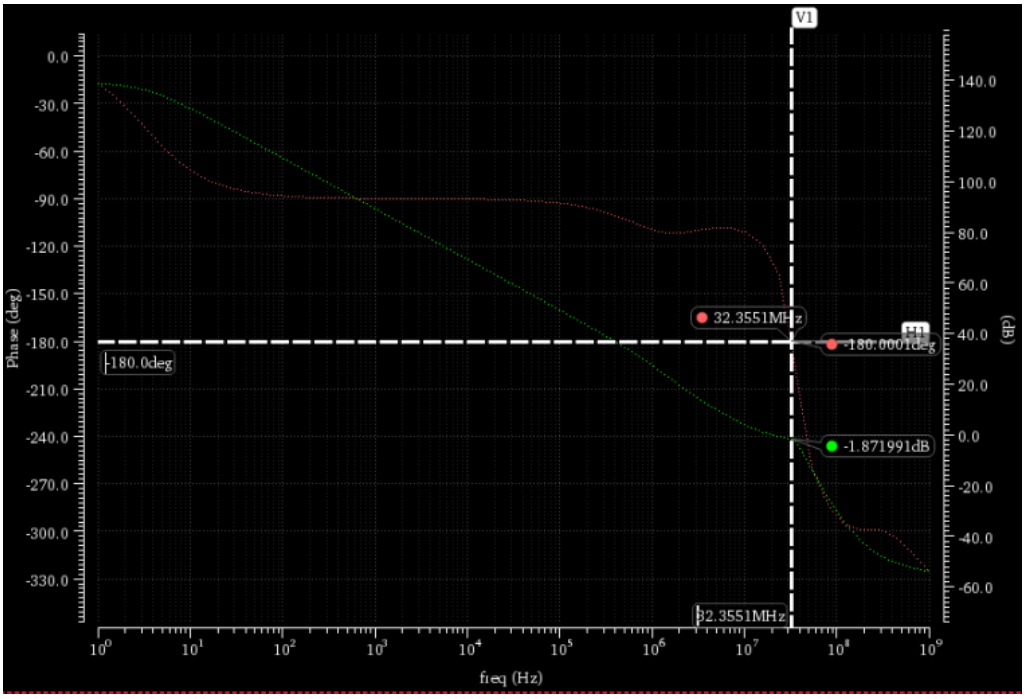

Fig. 4: Gain margin of the OPAMP

Without 5KΩ load resistor connected to the output, the DC voltage levels of the circuit is given in the below figure. The output DC level is tried to be set around 900mV, which is half of the V_{DD}. The obtained value is 899.8mV.

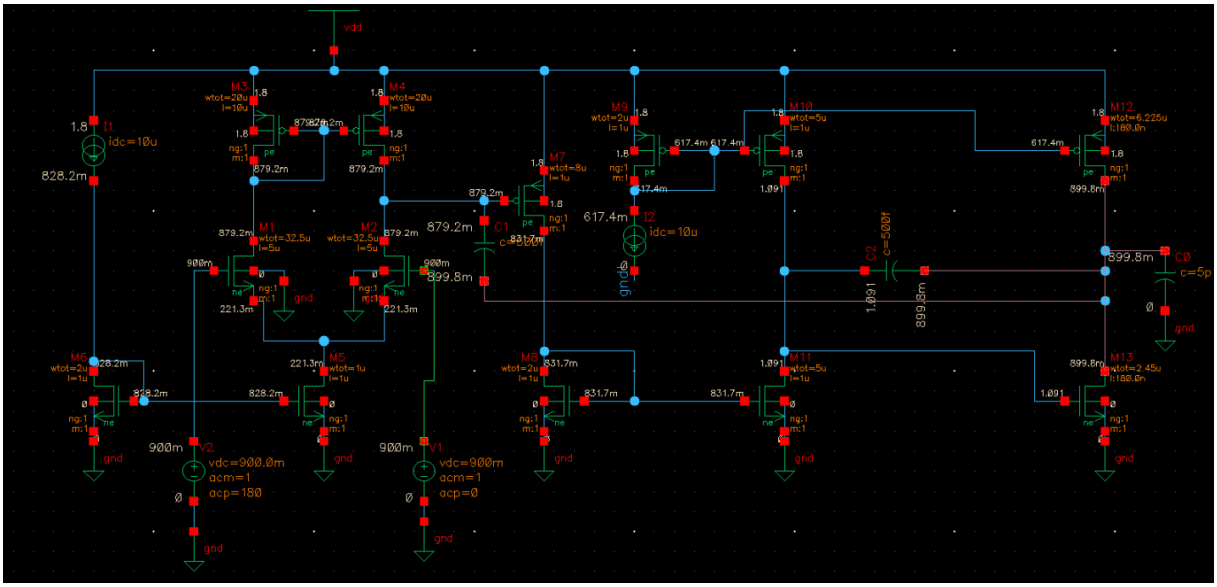

Fig. 5: DC node voltages of the OPAMP

With 5KΩ load resistor connected to the output, the DC voltage levels of the circuit is given in the below figure. One end of the 5KΩ load resistor is connected to 900mV supply and the other end is connected to the output of the OPAMP. As seen from Fig. 5 and Fig. 6, output DC levels are nearly the same value. The output DC level while driving resistive load is measured as 899.9mV.

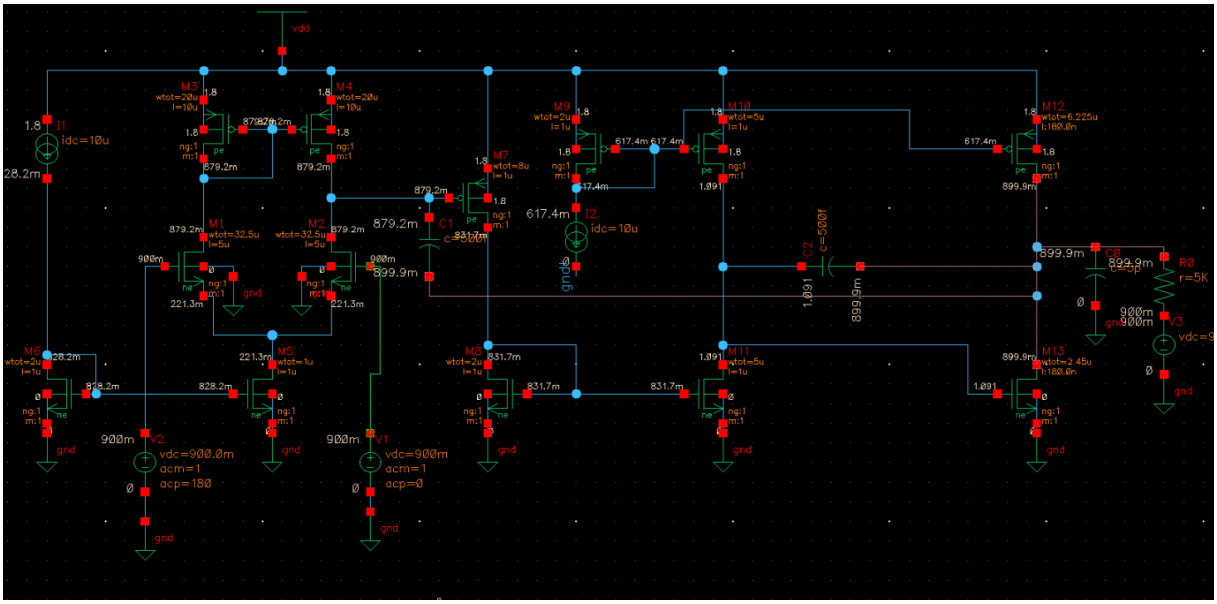

Fig. 6: DC node voltages of the OPAMP driving 5KΩ load resistor

The gain of the OPAMP when 5KΩ load resistor is connected is measured as 127dB which is greater than 100dB. Therefore the specification is satisifed also. Below figure shows the bode plot.

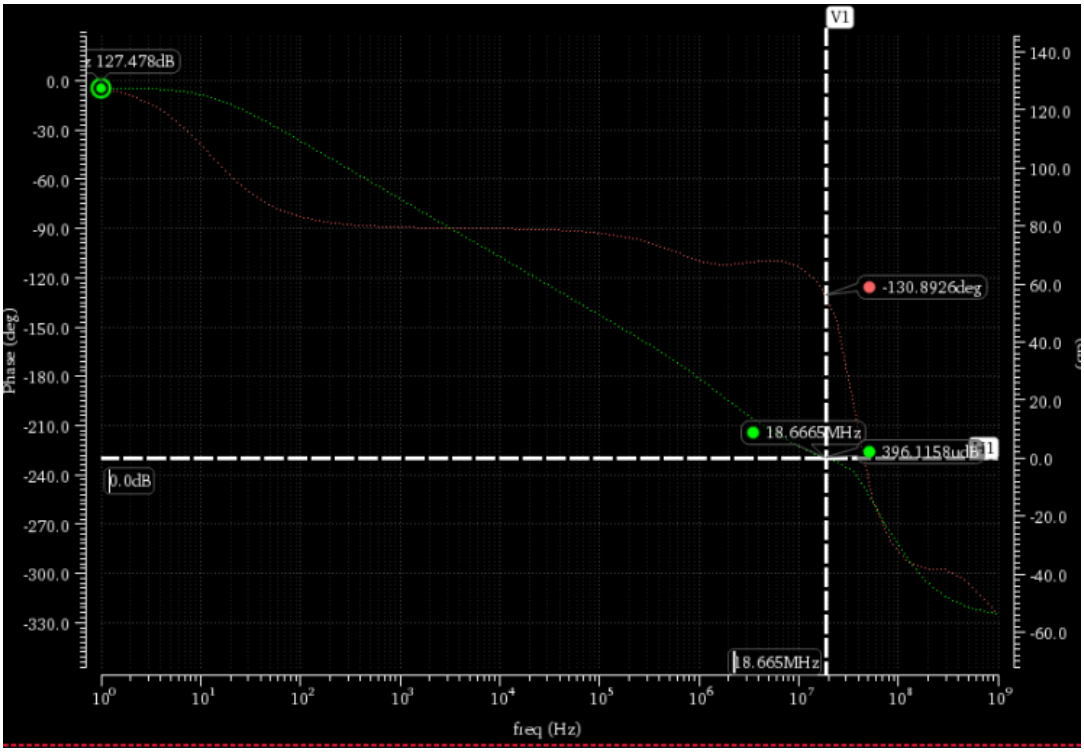

Fig. 7: AC gain of the OPAMP while driving 5KΩ load resistor

By using minimum length transistors at the final stage, R_{out} of the OPAMP is decreased significantly, therefore when 5KΩ resistor is connected, dB gain reduces from 138dB to 127dB. Also, the phase margin of the OPAMP while driving both resistive and capacitive load is measured as 49.11 degrees. The gain margin is measured as -3.46dB. The resistive load driving OPAMP is also stable as expected.

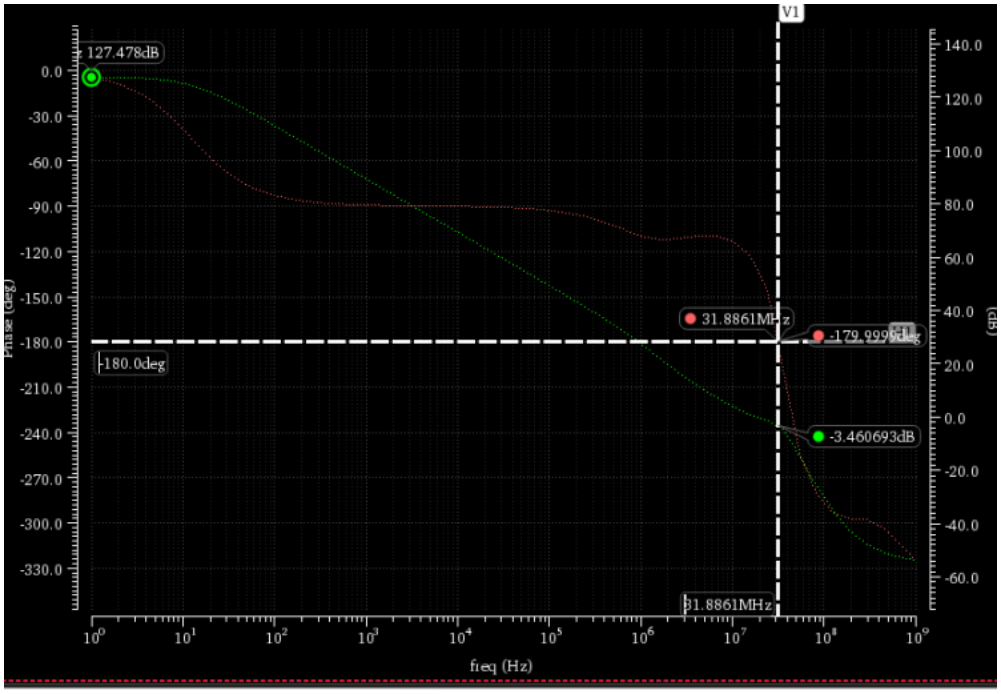

Fig. 8: Gain margin of the OPAMP driving resistive load

For the total power consumption of the circuit, basically all of the currents on the branches are summed up. The total current consumption of the OPAMP is calculated as 354.472 µA. Because the R_{out} of the final stage is too low, current is relatively higher there compared to other stages.

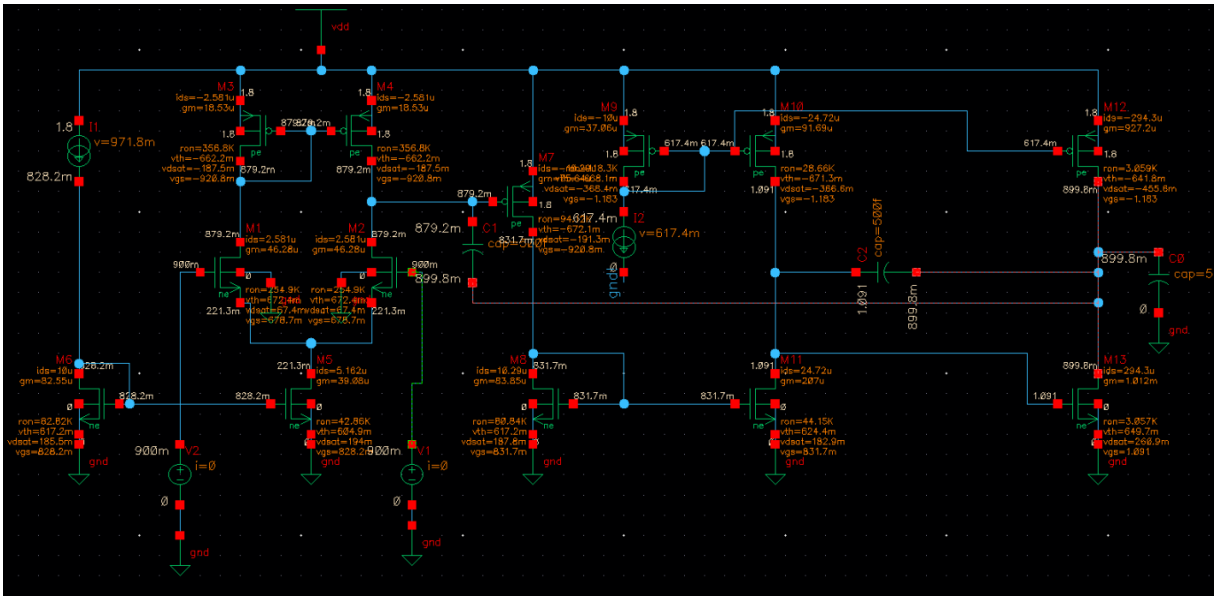

Fig. 9: Total current consumption of the OPAMP

Fig. 10 shows the closed-loop configuration of the OPAMP for voltage swing measurement. This configuration is a basic inverting OPAMP configuration with -5 gain.

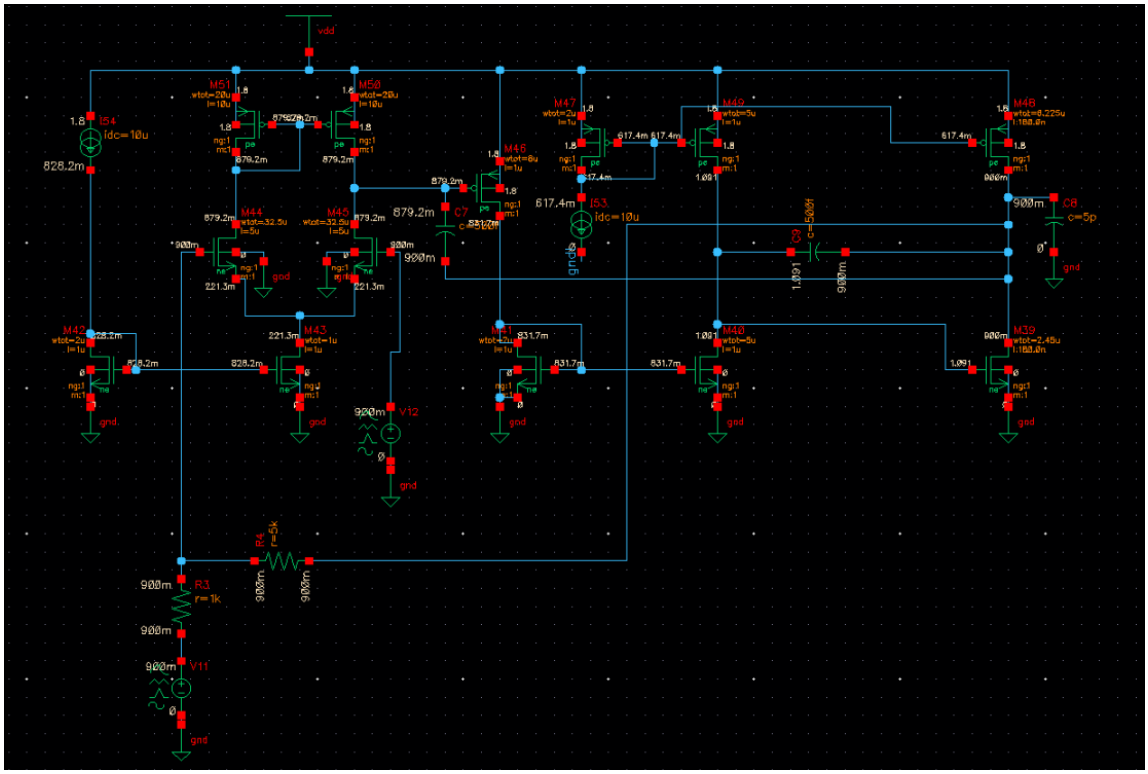

Fig. 10: Closed-loop inverting OPAMP configuration

The closed-loop voltage swing of the circuit is given in the figure below. The red-colored waveform represents the output voltage waveform, and the green-colored waveform depicts the input voltage, which is 100mV 10kHz sine wave. The output voltage is -5 times amplified version of the input voltage. The resulted voltage swing is in between 1.4V and 0.4V. Which satisfies the specification.

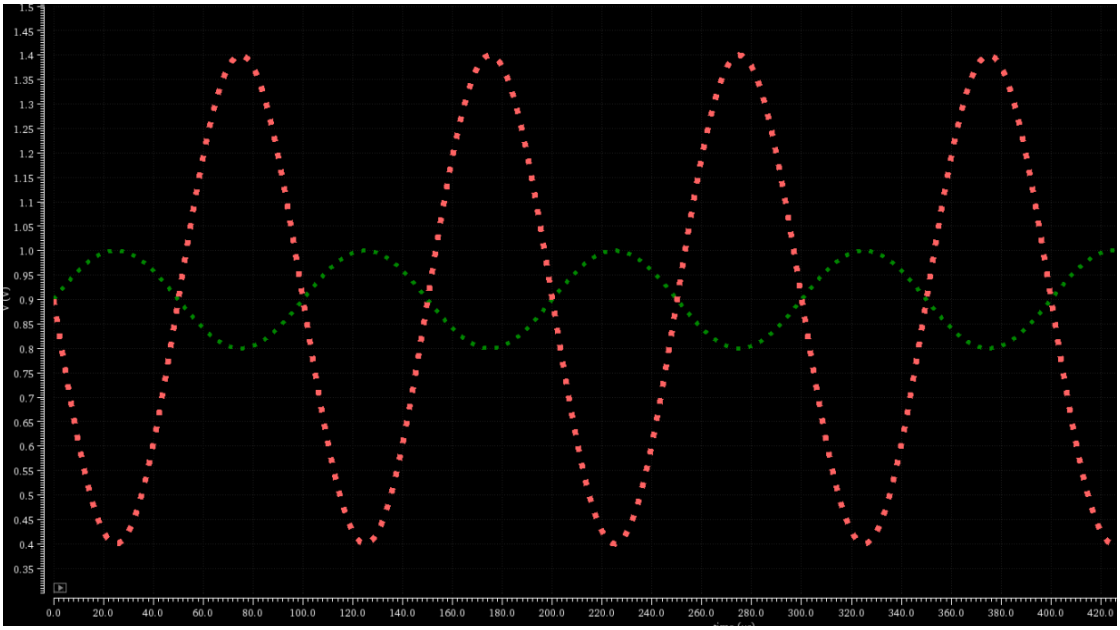

Fig. 11: Closed-loop voltage swing

Fig. 12 shows the test circuit for the noise.

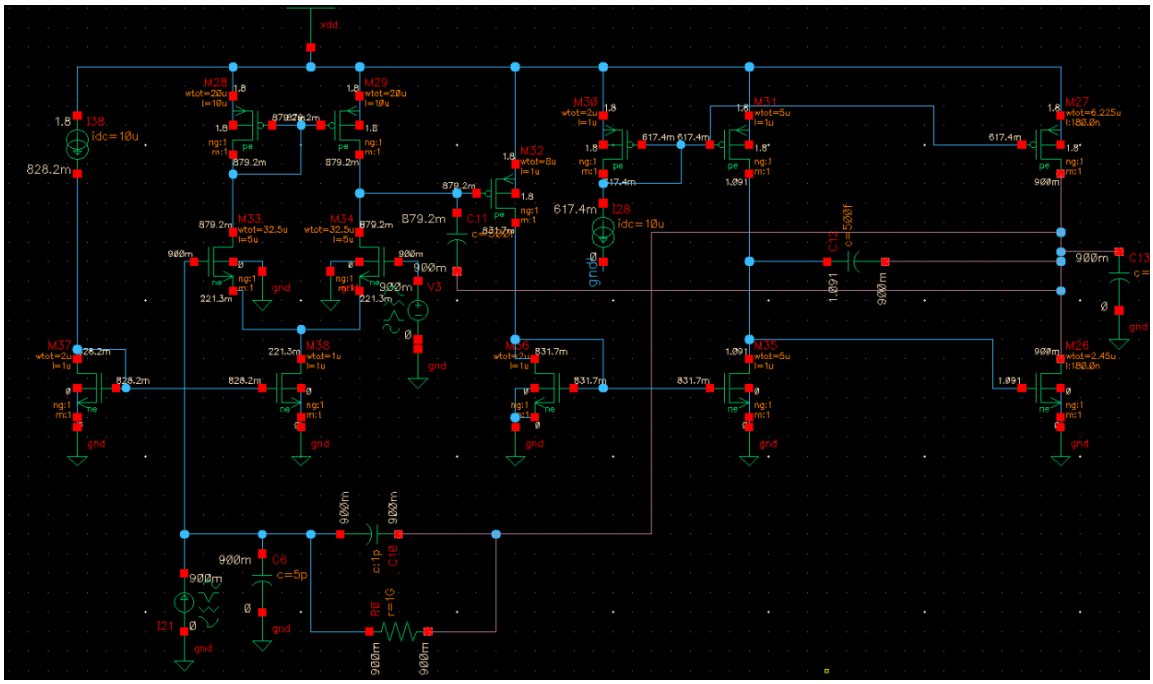

Fig. 12: Test circuit for the noise

The noise measurement circuit is built. According to specifications, a 15.9mV voltage swing must be seen. Fig. 13 shows the output voltage swing for the noise circuit. As seen from Fig. 13, the voltage swing is close to 15.9mV (915.63mV – 883.94mV), as expected.

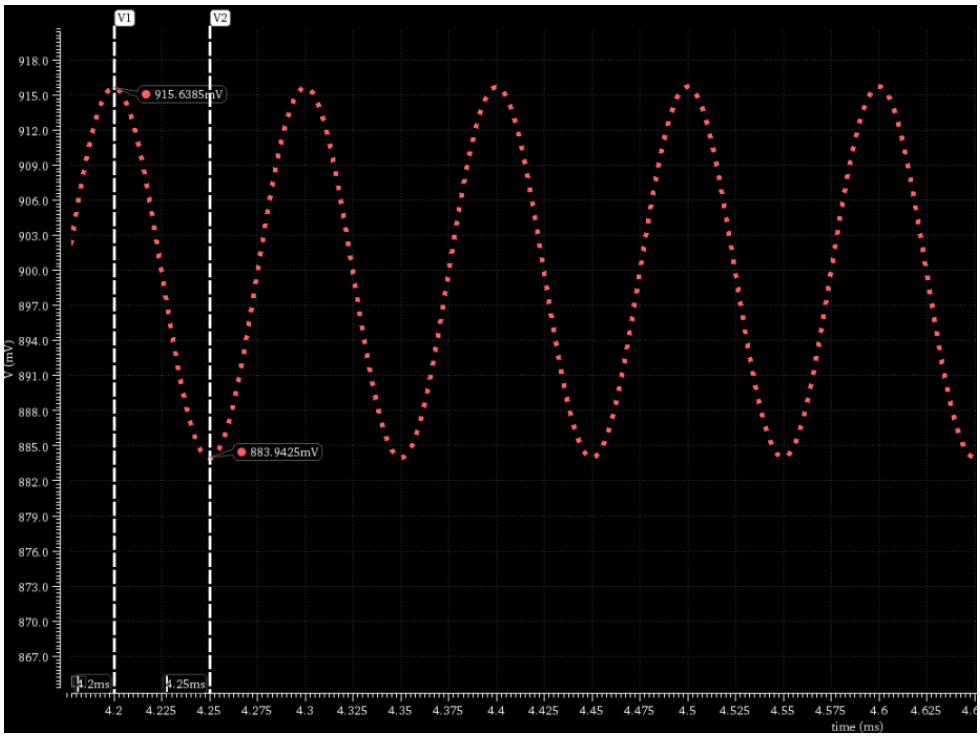

Fig. 13: Output voltage swing for the noise circuit

At 60nA, saturation begins, that is to say voltage swing becomes rail-to-rail (between 1.8V and 0V).

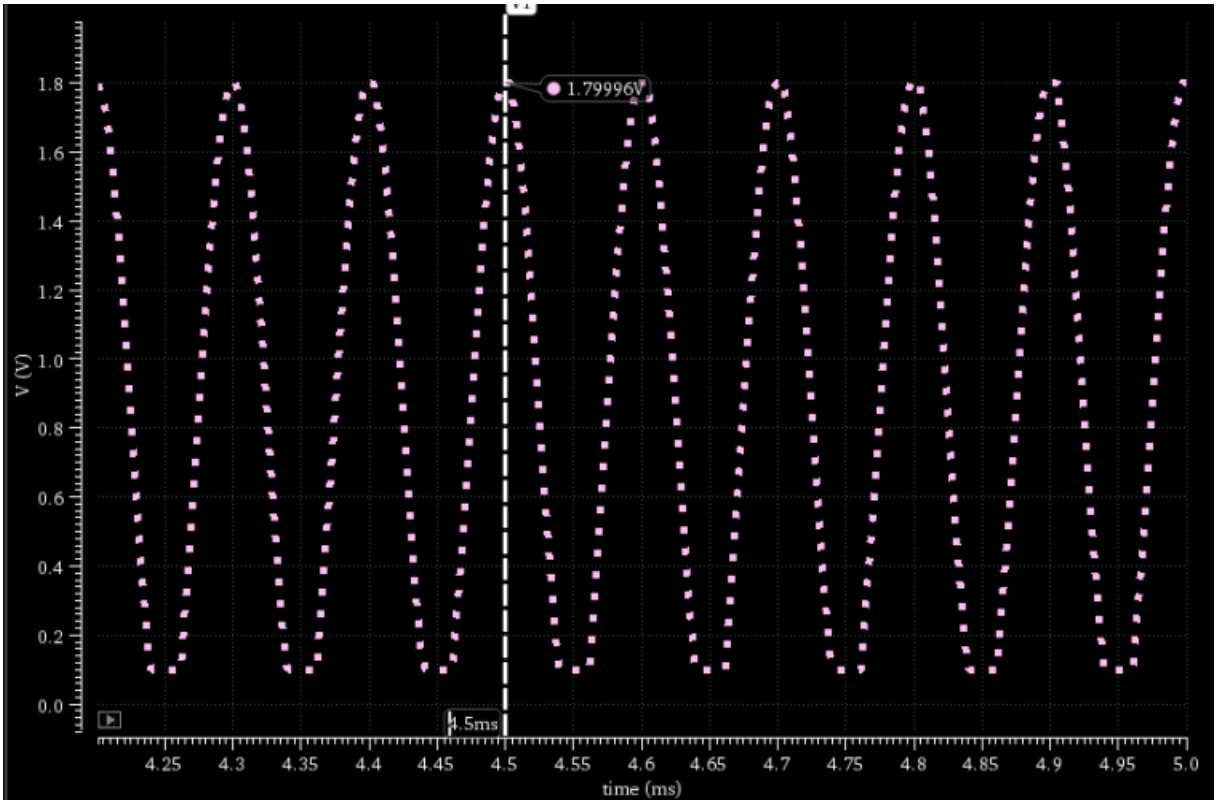

Fig. 14: Noise circuit saturated voltage swing

As mentioned earlier, the total noise contributor of the circuit is 5 transistor OTA. Fig. 12 shows the noise circuit and DC voltage levels.

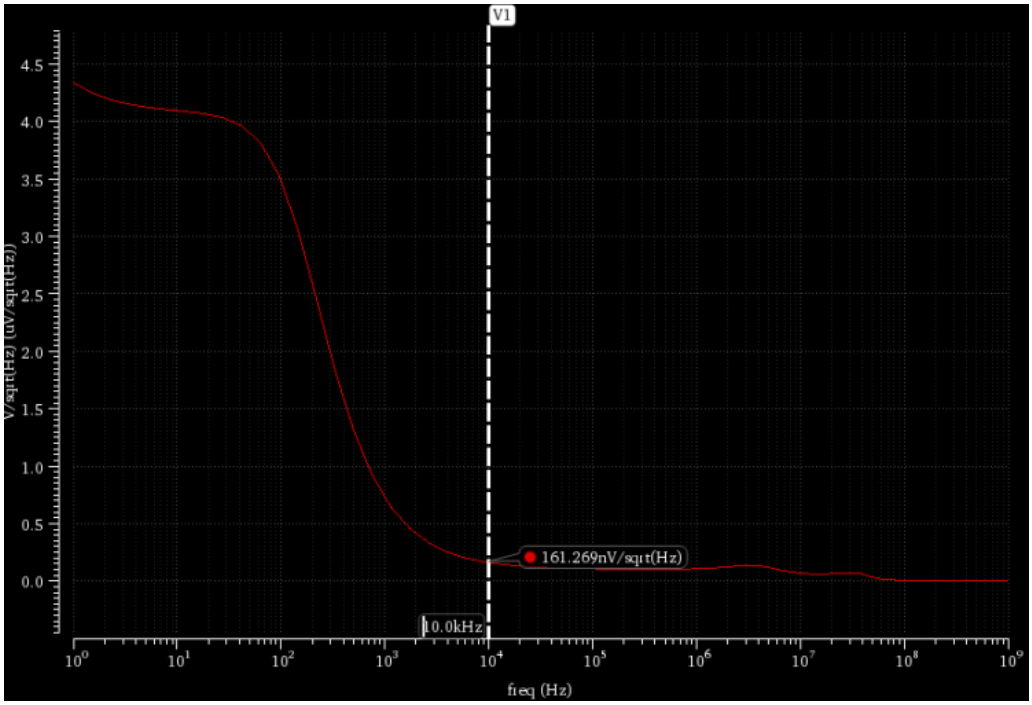

Fig. 15: Noise of the circuit at 10kHz

The total noise of the circuit is measured as 161.27nV at 10kHz (Fig. 14). In specifications, it is wanted as 60nV. This is the best value I achieved. As mentioned, W*L multiplication value plays an important role in the noise. Additionally, C_{gs} and C_{gd} are the ones that form C_{in}. The formula for the input capacitance C_{in} is given below. Because the gain is high, due to miller effect input capacitance is high also. 161.27nV is the best value that is achieved. The necessary formulas are given below.

$$Thermal\ noise = 4kT\gamma g_m$$

$$\frac{1}{f}\ (flicker)\ noise = \frac{K}{C_{ox}W * L} * \frac{1}{f}$$

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})$$

$$C_{gs} = \frac{2}{3}C_{ox}W * L$$

$$C_{in} = C_{gs} + (1 - gain) * C_{gd}$$

Looking at the above formulas, when L increases, noise will reduce, however, at the same time DC bias leveling highly depends upon W and L values. Additionally, due to the way of calculating the output noise, input capacitance is important. The value of the input capacitance is inversely related with the L. Therefore finding W and L values which satisfies all three of the conditions are difficult enough.

Conclusion: All of the specifications expect the noise are satisfied. Because there are various topologies of OPAMP designs, telescopic OPAMP may result in a lower noise result compared to nested miller-compensation based OPAMP due to relatively smaller miller effect. (Miller effect gain is larger in 5 transistor OTA than telescopic OPAMP, due to common source configuration).

Table 1: Comparison of the design specifications

	Project Specifications	**Designed Circuit Specifications**
Noise	<60 nV/√Hz @10kHz	161.27nV at 10kHz
Current consumption	<1mA	354.472 µA
Unity-Gain Bandwith	>10MHz	15.79 MHz
dB gain without 5KΩ load	>100dB	138dB
dB gain while driving 5KΩ load	>100dB	127dB
Voltage Swing	1.4V – 0.4V	1.4V – 0.4V

Layout: Layout of the schematic is designed.

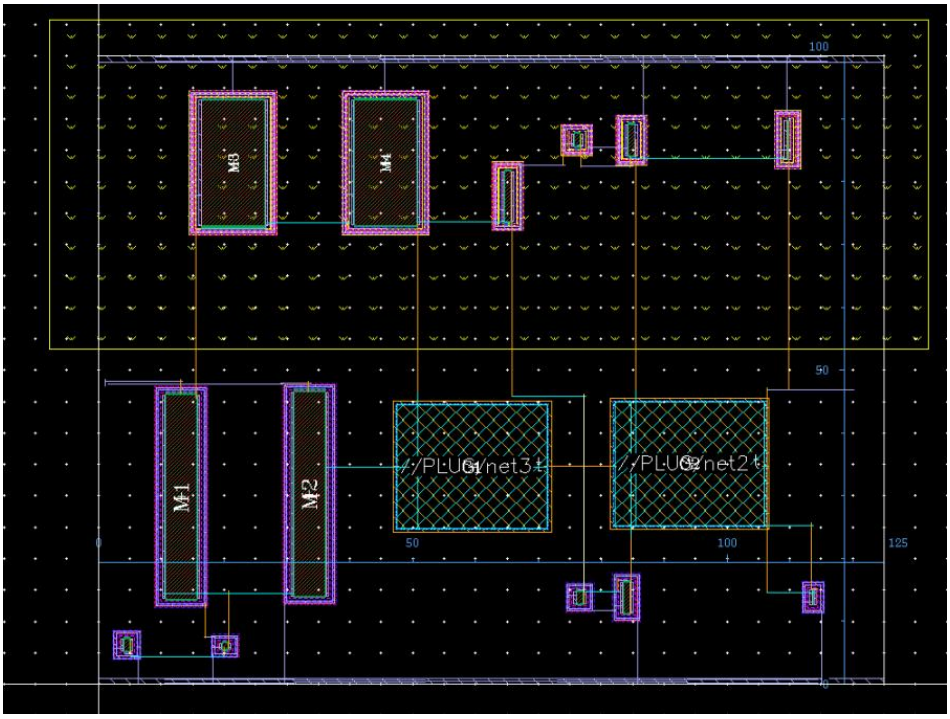

Fig. 16: Layout

As seen, 500fF capacitors are huge compared to the sizes of the transistors. The height is 100µm and width is 125µm. It can be smaller but in order not to squeeze the area due to capacitors, 125µm is considered as rational. Vin+ and Vin+ input pins are located at the left side and output pin is located at the right side. V_{DD} rail is located at the top with height 1µm, so as GND, which is located at the bottom of the cell.

Fig. 17 and Fig. 18 shows that the design is DRC and LVS error-free.

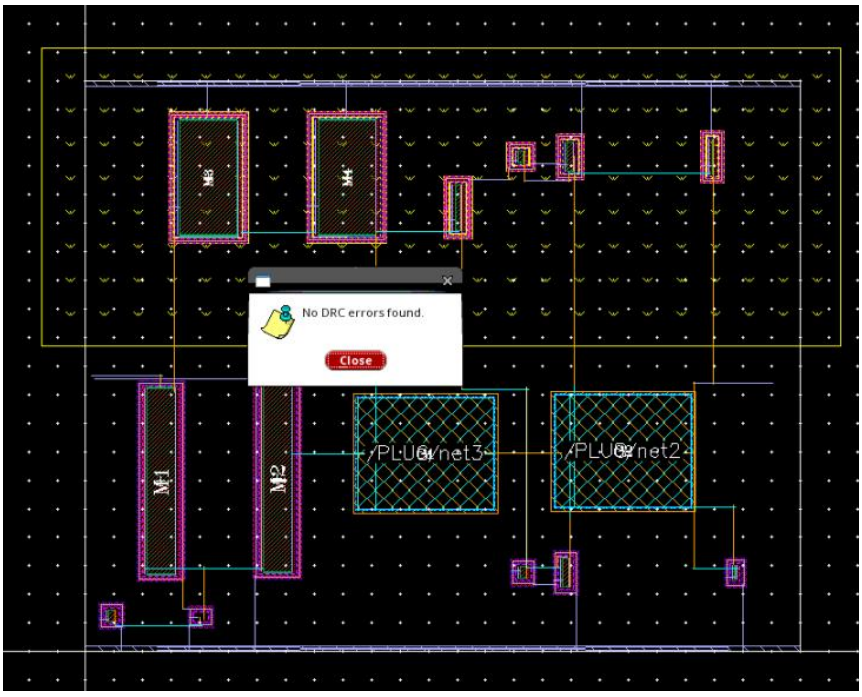

Fig. 17: DRC error-free

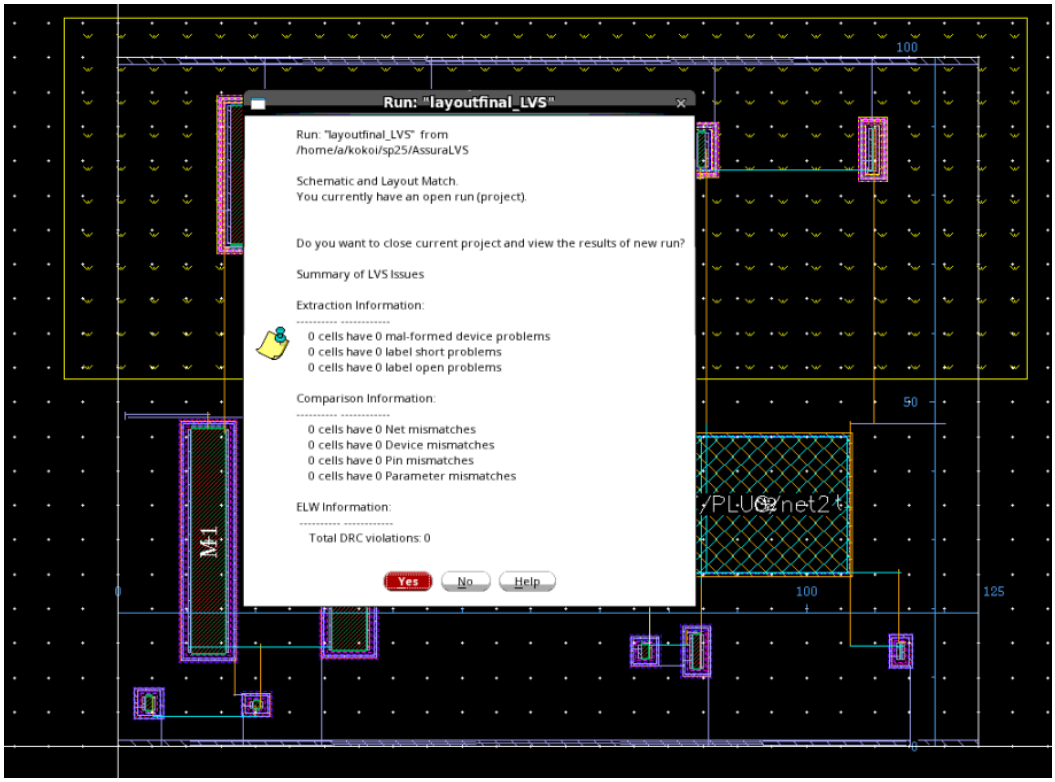

Fig. 18: LVS error-free