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EEE415 Homework #2

Introduction:

The purpose of this assignment is to compare simulation results of Cadence with the formulas that are derived in the class. In the last part of the assignment, a single stage amplifier with given specifications wanted to be designed.

Analysis:

Part 1)

By looking at the datasheet of the ne, NMOS transistor, it is written that V_{TH}=0.58V. However, in the Cadence, V_{TH} value is turned out to be 0.628V. To achieve a value close to 100mV (103mV) as V_{OV}, I defined the V_{GS} voltage as 0.73V. V_{DS} voltage is defined as 1.8V, which is the maximum allowable voltage. Bulk and source are conencted to ground. Fig. 1 shows the circuit schematic.

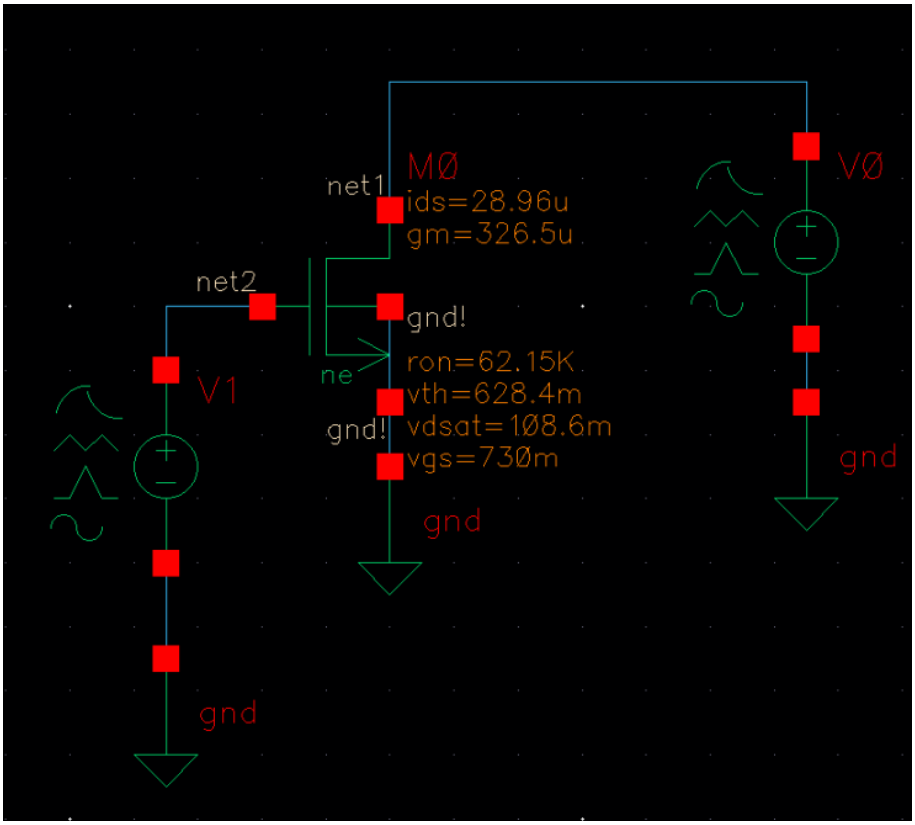

Fig. 1: Part 1 circuit schematic

According to the DC simulation, here are the results:

- V_{TH} = 628mV

- $r_o = \frac{1}{gds}$ = 134.4 KΩ
- $\mu_n * C_{ox}$ = 3.42*10^{-4}

gds	7.443u
gm	326.5u
id	29u
ids	28.96u
isub	35.39n
ron	62.15K
vbs	0
vds	1.8
vdsat	108.6m
vgs	730m
vth	628.4m

Fig. 2: NMOS characteristics

In Cadence, betaeff value is the following parameter: $\mu_n * C_{ox} * (W/L)$. The betaeff value is mesaured as 3.798m in Cadence.

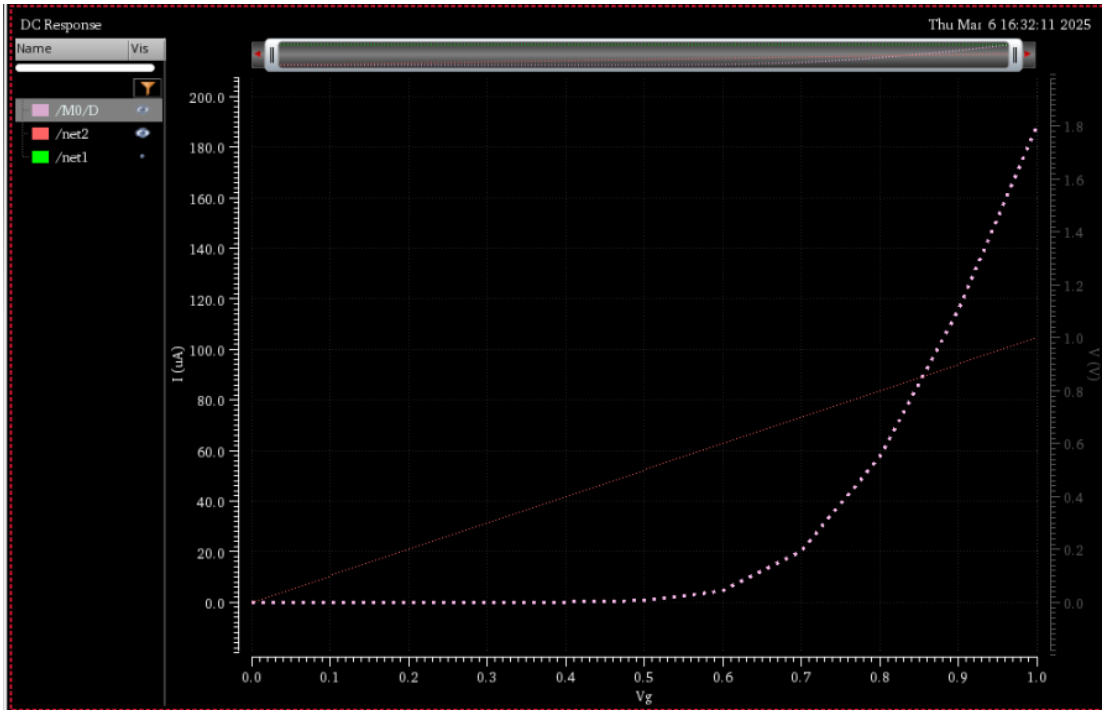

Fig. 3: Drain current of the NMOS

For parametric sweep, I choose a gate-to-source voltage V_{GS} from 0V to 1V.

As $V_{GS} < V_{TH}$, NMOS is OFF, therefore the current I_D is very close to 0. To ensure the equation holds with the simulation, I will take the case where V_{GS} = 0.73V. Using (Eqn. 1), the value of I_D's will be compared.

$$I_D = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})(V_{GS} - V_{th})^2 \quad \text{(Eqn. 1)}$$

At 730mV, according to the simulation results, I_D = 28.96µA. The calculated I_D is 19.76µA. As seen from the results, the values are close to each other with a slight difference, so the equation holds with the simulation and analysis.

Part 2)

For PMOS, source is directly connected to 1.8V supply, and gate is conencted to 1.07V supply, to achieve V_{GS} = -0.73V. Drain is connected to GND. V_{OV} = 96mV (~100mV). With these values, according to the DC operation, here are the results:

- V_{th} = -633.9mV
- $r_o = \frac{1}{gds}$ = 1.7 MegaΩ
- $\mu_p * C_{ox} = 6.498 * 10^{-5}$

gds	587.4n
gm	69.7u
id	-5.227u
ids	-5.227u
isub	-84.9p
ron	344.4K
vbs	0
vds	-1.8
vdsat	-121m
vgs	-730m
vth	-633.9m

Fig. 4: PMOS characteristics

When V_{GS} = -0.73V, drain current I_D = 5.23µA, whereas using the equation, the calculated value for drain current is 3.33µA. As expectedi the calculated and measured values are slightly similar.

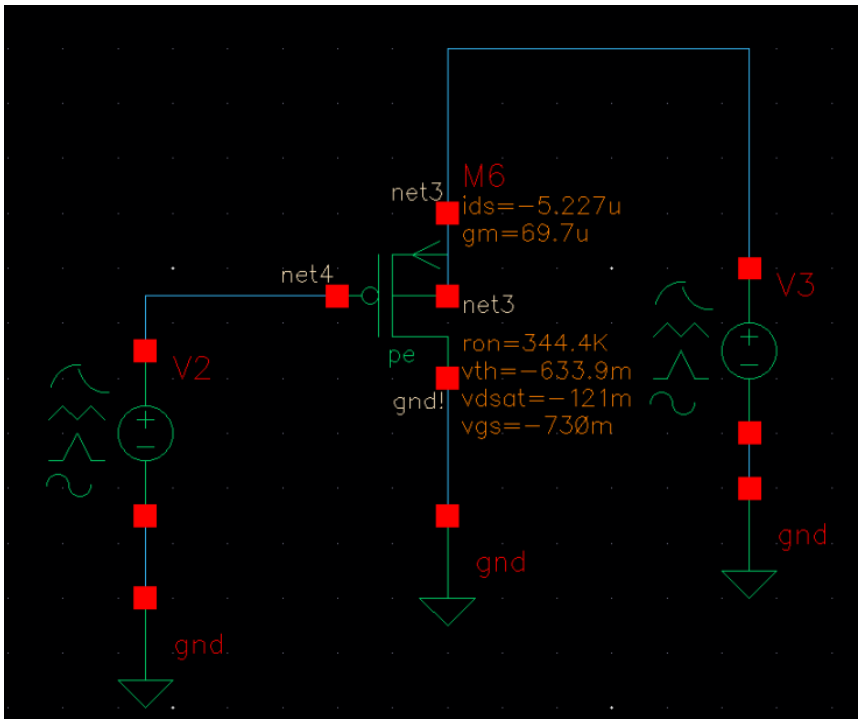

Fig. 5: PMOS circuit schematic

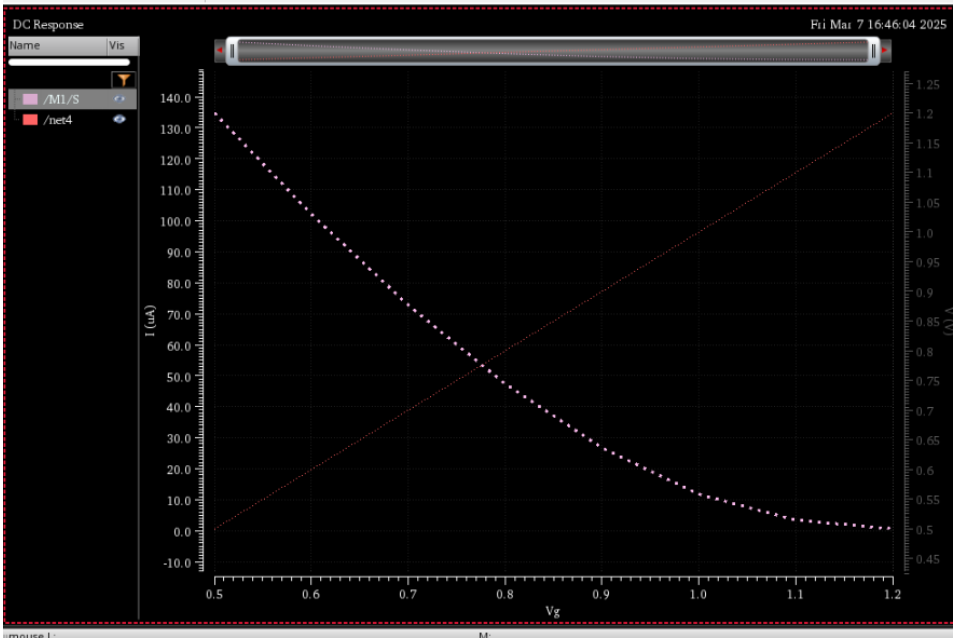

Fig. 6: PMOS I-V characteristics graph

Above figure shows the relation between V_G and drain current I_D. While V_G increases, V_{GS} decreases, therefore the drain current is downwardly sloping in this graph.

Part 3)

In this final part, I designed a single-stage amplifier which satisfies the following design specifications:

- $|A_V|>100$
- Total current consumption <0.1mA
- Peak to peak voltage swing at the output >1.2V

I used a PMOS at the top and a NMOS at the bottom, below figure shows the circuit schematic. None of the transistor have body effect in this configuration.

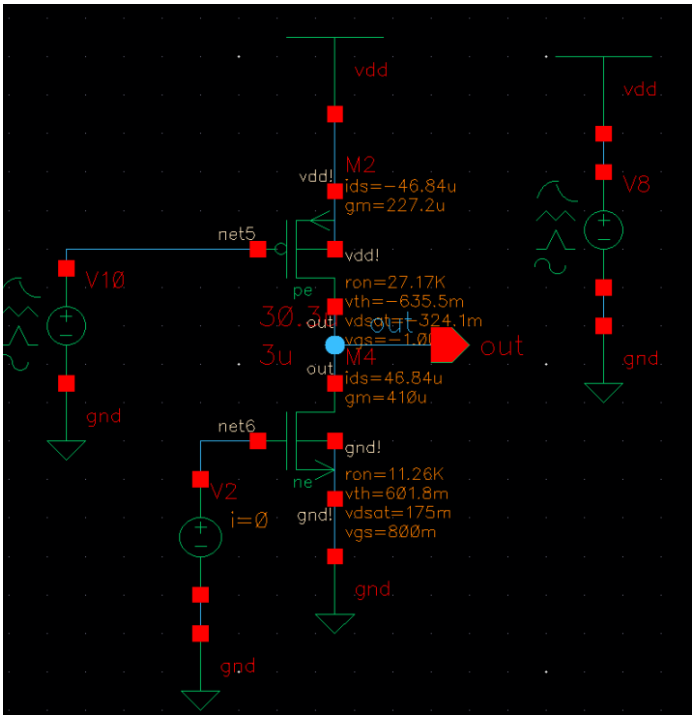

Fig. 7: Part 3 circuit schematic

As seen from the rough analysis, gain of this amplifier is calculated as $A_V = gm_1(r_{o1}//r_{o2})$.

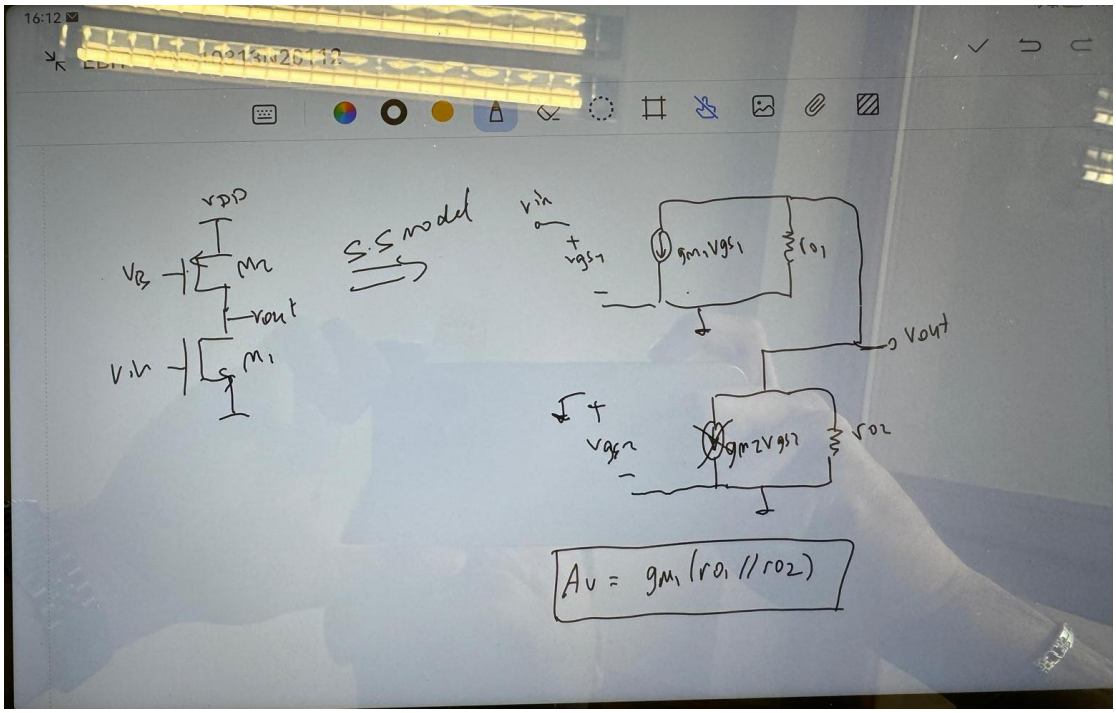

Fig. 8: Rough analysis of the single-stage amplifier

Fig. 9 shows the results for PMOS and Fig. 10 shows the results for NMOS transistors.

gds	3.492u
gm	227.2u
id	-46.84u
ids	-46.84u
isub	-175.5f
ron	27.17K
vbs	0
vds	-1.273
vdsat	-324.1m
vgs	-1.005
vth	-635.5m

Fig. 9: Results for PMOS

gds	533.8n
gm	410u
id	46.84u
ids	46.84u
isub	353.9a
ron	11.26K
vbs	0
vds	527.4m
vdsat	175m
vgs	800m
vth	601.8m

Fig. 10: Results for NMOS

I named PMOS as M2 and NMOS as M1. So here are the r_o values:

- r_{o1} = 1.87 MΩ
- r_{o2} = 286.3 KΩ

According to the gain formula, inserting these r_o values and gm_1, corresponding calculated gain turned out to be A_v = 101.84 whereas in the simulation, the gain value is measured as 101.85 (Fig. 11).

I used an external DC source for the gate of the PMOS, because when I directly connect the gate to drain, gain is reduced. The gate voltage PMOS is determined as 795mV, and gate voltage of the NMOS is determined as 800mV. The size of the PMOS is not changed, which is W=2µm and L=180nm. However, to achieve a gain higher than 100, I resized the NMOS as W=30.3µm and L=3µm. I achieved these values by trial and error looking at the gain graph. This circuit's current consumption is 46.84µA, which is below the limit (100µA).

As seen from Fig. 11, a gain of 101.85 is achieved. For the voltage swing condition, transient analysis was performed.

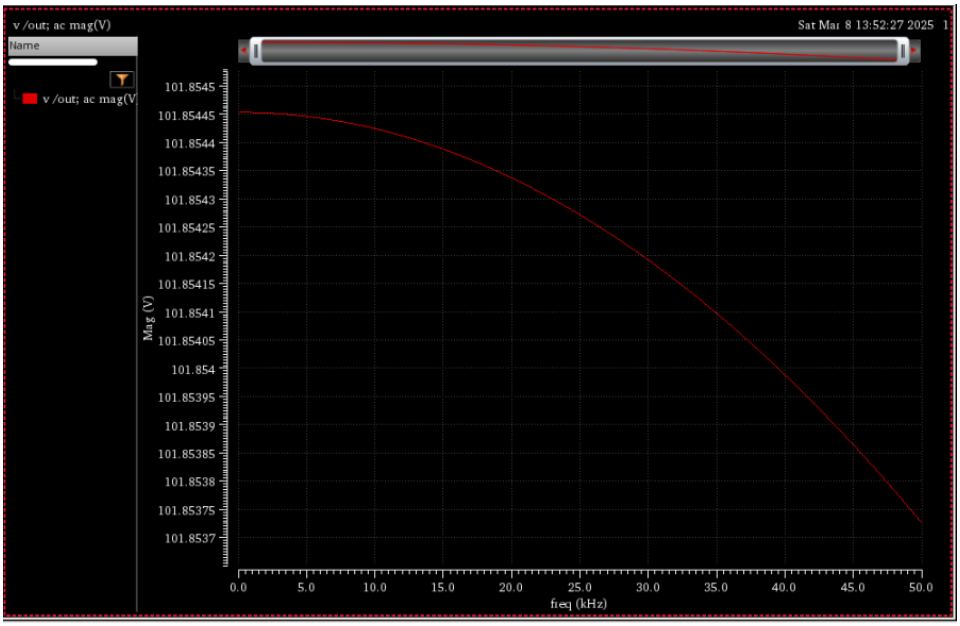

Fig. 11: Gain of the amplifier

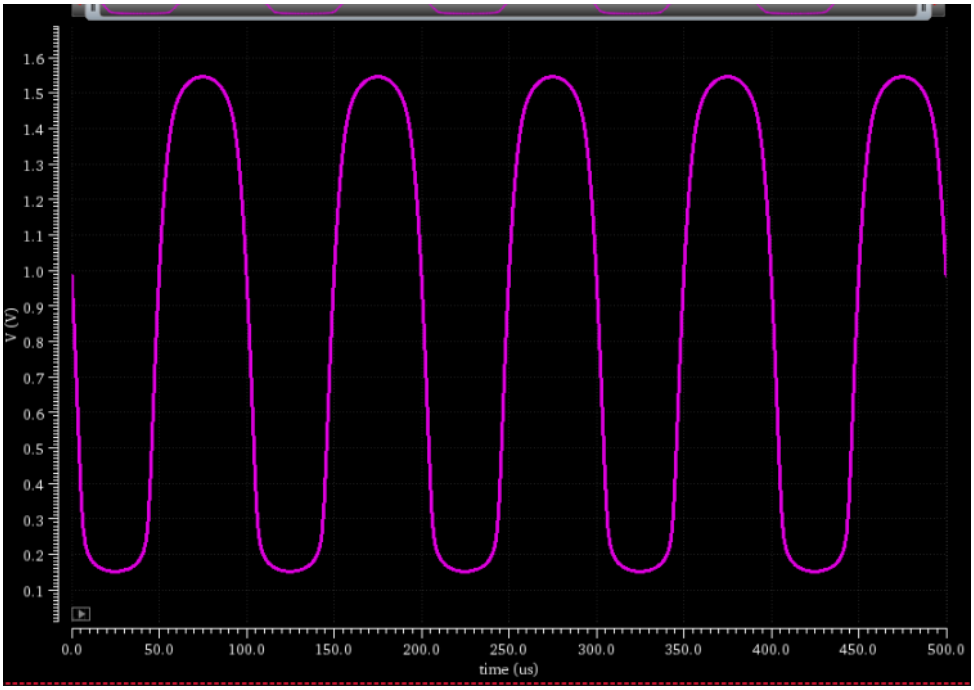

Fig. 12: Output voltage swing

Looking at the above figure, it is seen that a voltage swing around 1.6V is achieved. The minimum voltage is 0.15V and maximum voltage is 1.54V, as measured. According to the specifications, the swing should be larger than 1.2V, therefore this specification is also satisfied.