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EEE415 Homework #3

Introduction:

The goal of this assingment is to design a nMOS input cascode with a cascode pMOS current source load. The gain, $|A_V|$ should be greater than 500 and 3dB bandwith should also be greater than 3MHz. The layout of the designed amplifier will also be drawn.

Analysis:

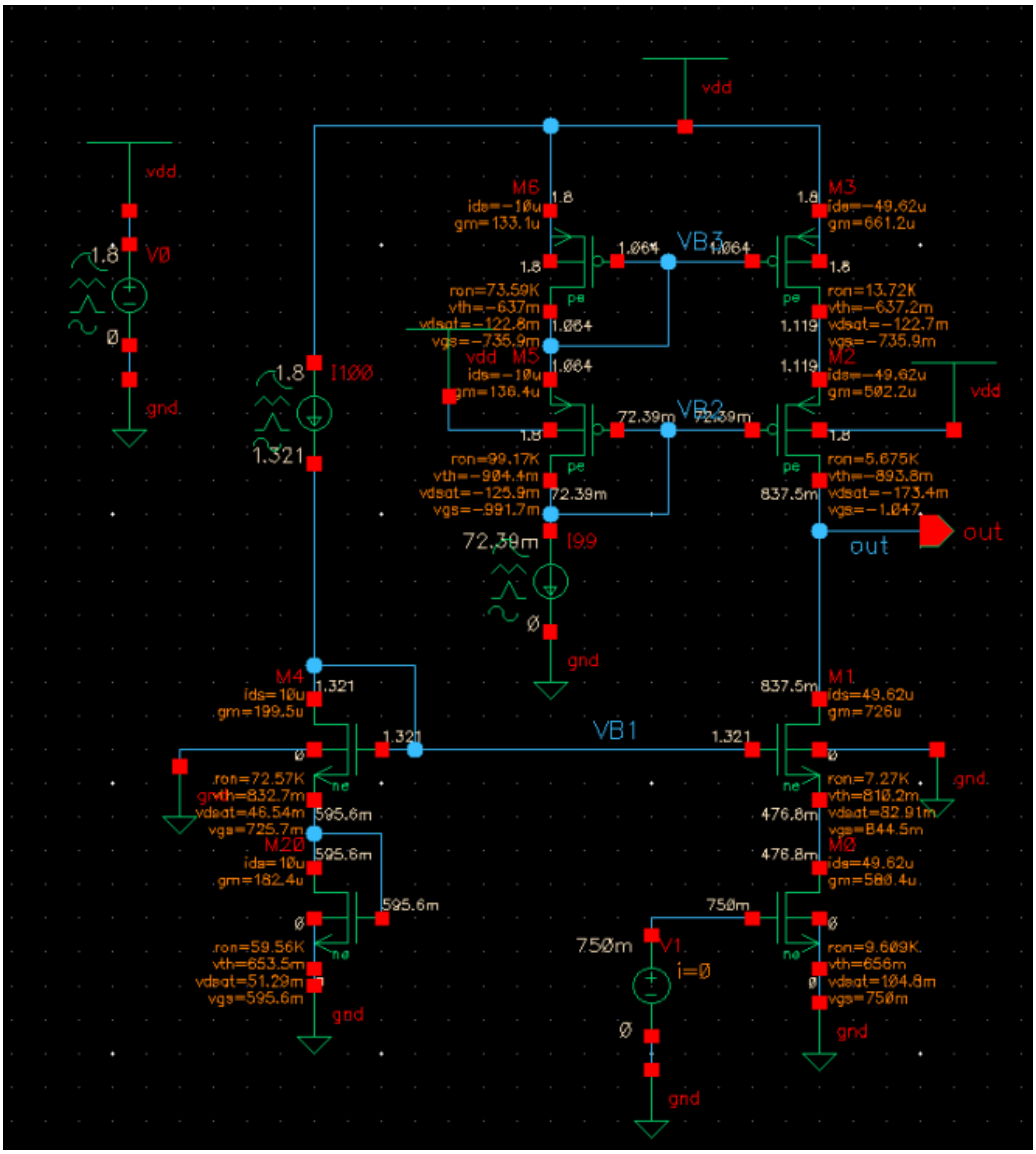


Fig. 1: Designed amplifier

The rightmost part is the nMOS input cascode with a cascode pMOS current source load. To provide bias voltages to these transistors, two separate current mirror branches are designed, one for nMOS one for pMOS. The main logic of the current mirror is using a reference current and diode connected transistor to get a gate voltage and mirror the current to the actual branch.

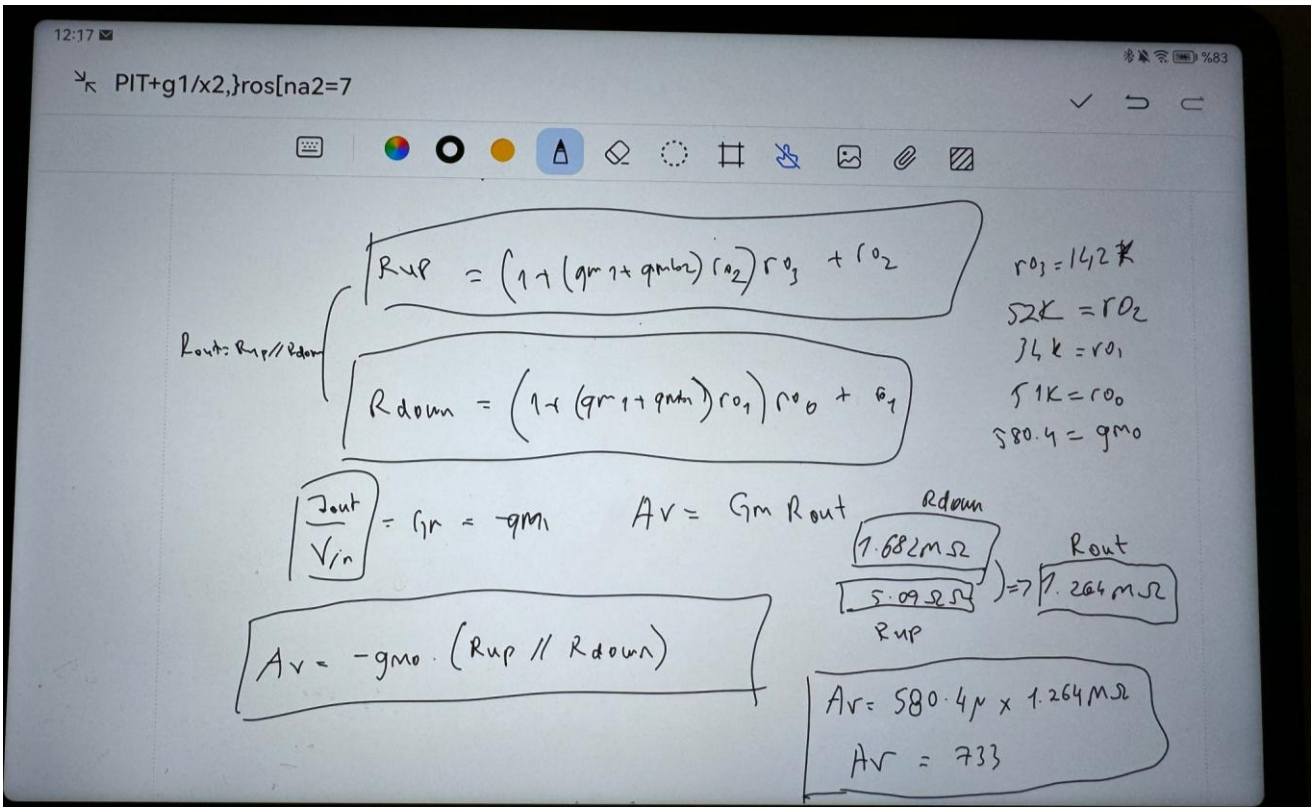
The reference current is given as 10µA. The amplifier is specified as 50µA, therefore the W for the amplifier is 5 times the current mirror branch. The obtained current flowing on the amplifier is 49.62µA as specified.

The biasing voltages are found with trial and error in general. The general logic relied on is when W increases, current drop from drain to source decreases. This helped a lot. Also the logic between V_{GS} and W considered to determine biasing voltages.

As specified, DC output at the output voltage is measured as 837.5mV, which is in the range (0.8V – 1V).

While determining the biasing voltage for the nMOS transistor, 2 transistors were needed to get the desired 1.3V bias voltage. Therefore an additional diode connected nMOS is used.

The analysis for the gain of the circuit can be seen in below figure.



The g_m, g_{mb}, and r_o ($1/g_{ds}$) values for the amplifier transistors are listed below:

- g_{m2} = 502.2µ
- g_{mb2} = 160.8µ
- g_{m1} = 726µ
- g_{mb1} = 192.6µ
- g_{m0} = 580.4µ

- r_{o3} = 142KΩ
- r_{o2} = 52KΩ
- r_{o1} = 34KΩ
- r_{o0} = 51KΩ

string	OP("/M3" "??")
gds	7.006u
gm	661.2u
id	-49.62u
ids	-49.62u
isub	-5.157a
ron	13.72K
vbs	0
vds	-680.9m
vdsat	-122.7m
vgs	-735.9m
vth	-637.2m

Fig. 2: M3 pMOS operating points

string	OP("/M2" "??")
gds	19.18u
gm	502.2u
id	-49.62u
ids	-49.62u
isub	-1.117a
ron	5.675K
vbs	680.9m
vds	-281.6m
vdsat	-173.4m
vgs	-1.047
vth	-893.8m

Fig. 3: M2 pMOS operating points

string	OP("/M1" "??")
gds	29.16u
gm	726u
id	49.62u
ids	49.62u
isub	576.2a
ron	7.27K
vbs	-476.8m
vds	360.7m
vdsat	82.91m
vgs	844.5m
vth	810.2m

Fig. 4: M1 nMOS operating points

string	OP("/M0" "??")
gds	19.55u
gm	580.4u
id	49.62u
ids	49.62u
isub	769.2a
ron	9.609K
vbs	0
vds	476.8m
vdsat	104.8m
vgs	750m
vth	656m

Fig. 5: M0 nMOS operating points

The formula for the gain is given in the below equation:

$$|A_v| = G_m R_{out} = g_{m0}[(1 + (g_{m1} + g_{mb1})r_{o1})r_{o0} + r_{o1})//(1 + (g_{m2} + g_{mb2})r_{o2})r_{o3} + r_{o2})]$$

$$|A_v| = 580.4\mu * (1.682M\Omega//5.09M\Omega) = 733$$

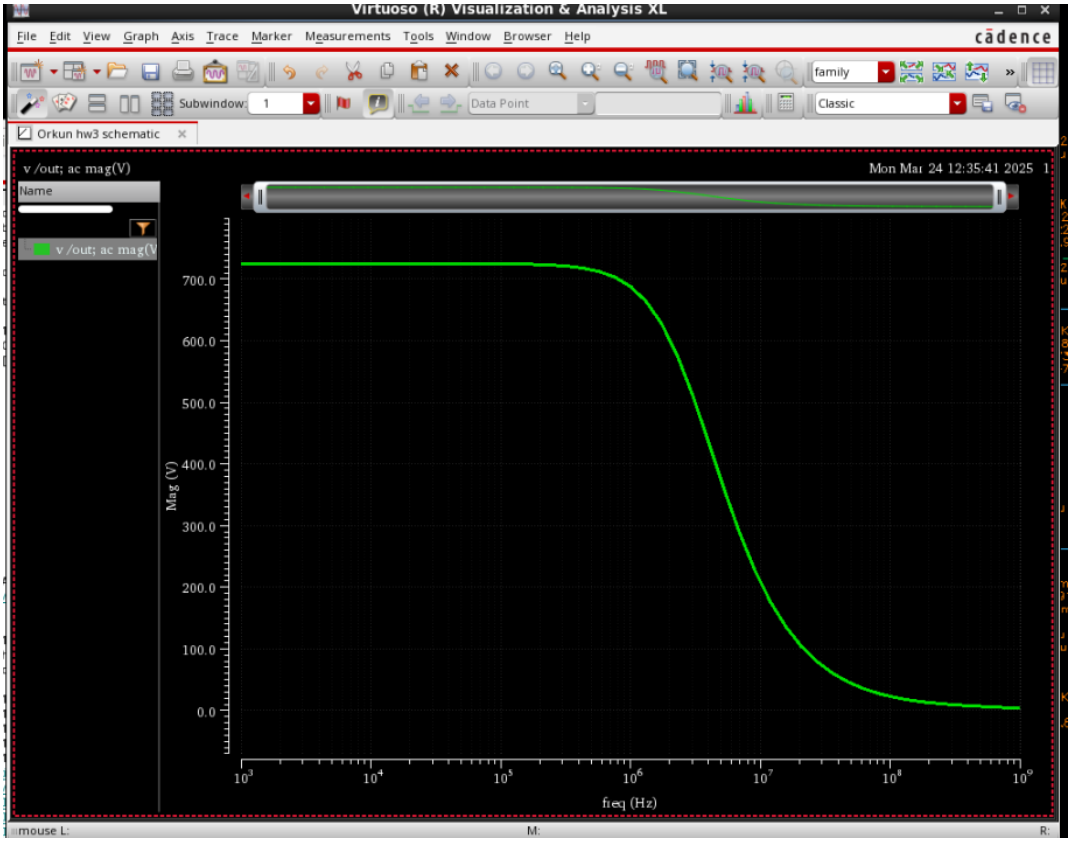


Fig. 6: Gain of the amplifier

As seen from the graph and mathematical calculation, the results are similar to each other. According to the graph, the gain is measured as 725 (V_{out} = 725V when V_{in} = 1V AC). Therefore, this amplifier satisfies the gain condition, which has to be greater than 500. For the 3dB bandwith point, I multiplied the gain of the circuit with 0.707 (1/sqrt2). The point is calculated as 512.575V.

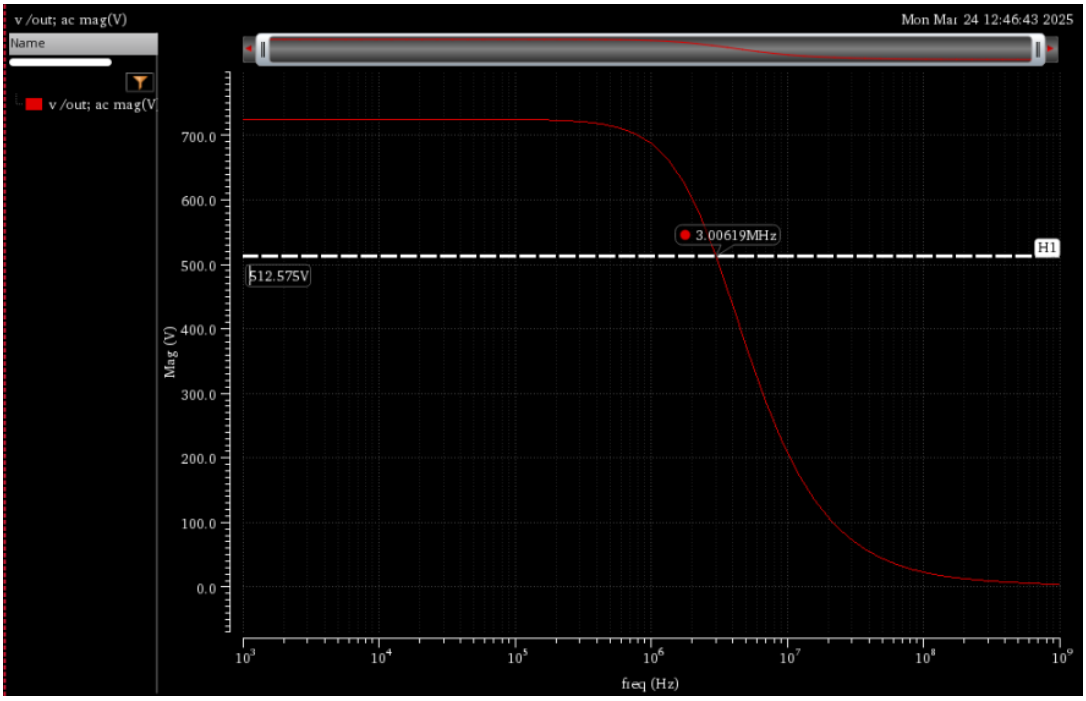


Fig. 7: 3dB bandwith point

The 3dB bandwith is measured a 3.062MHz, which is greater than 3MHz. Therefore bandwirh specification is also satisfied. As an additional information, due to the fact that gain-bandwith product is fixed, gain of the circuit is reduced a bit to obtain a bandwith greater than 3MHz.

To generate this much gain, width of the transistors are crucial. Even the width of one of the transistors is played, the gain reduces significantly.

To analyze whether there is a linear relation between V_{in} and V_{out}, I did DC-sweep analysis for V_{in} from 700mV to 800mV and commented on the results.

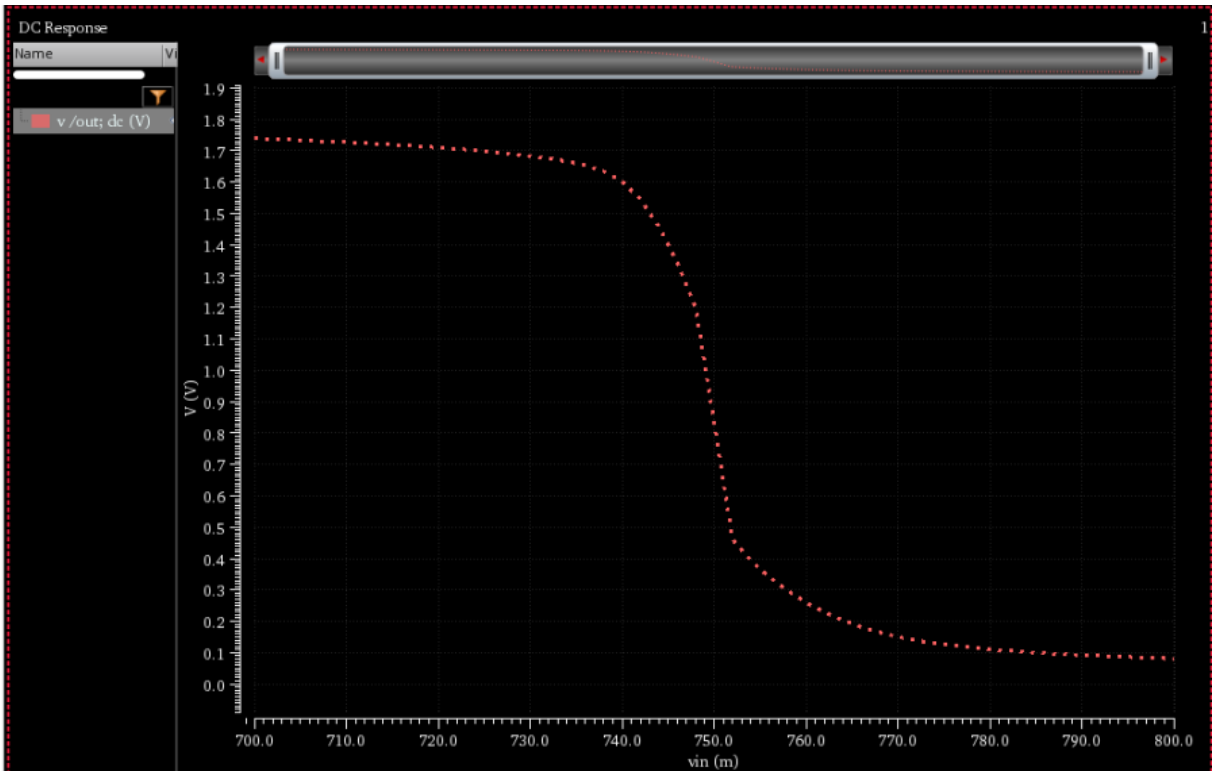


Fig. 8: Linearity relation between V_{in} and V_{out}

As seen from the above figure, V_{in} and V_{out} does not have a linear relation between each other. As V_{in} increases above 740mV, a significant decrease observed at the V_{out} voltage.

Fig. 9 shows the transient respone of the amplifier.

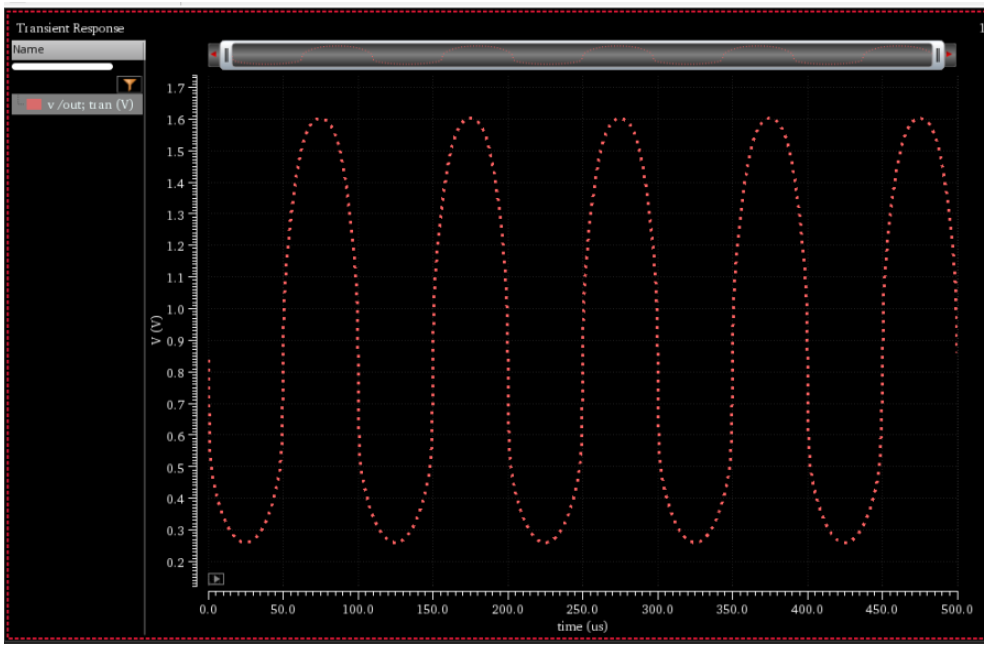


Fig. 9: Transient response

The voltage swing at the output is near 1.4V

The input referred noise graph of the amplifier can be seen in below figure.

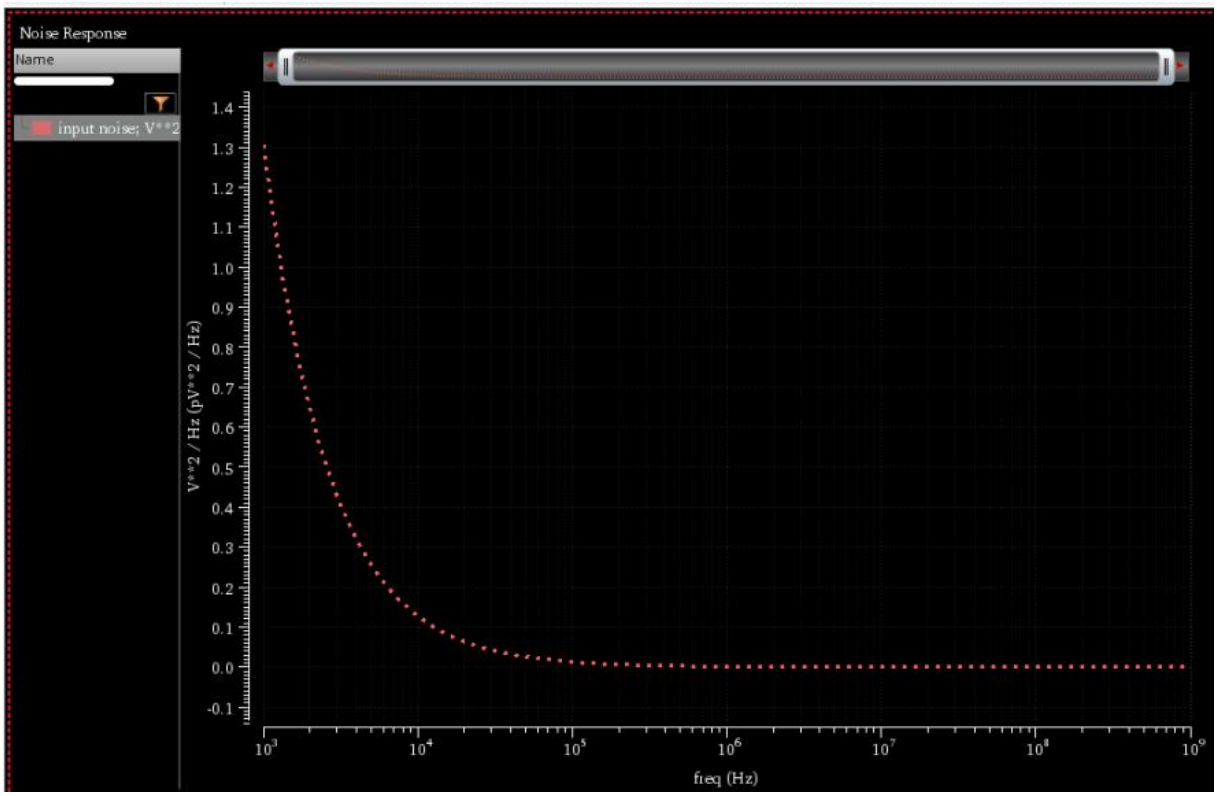


Fig. 10: Input referred noise

The input referred noise is given in pV**2/Hz units. As frequency increases, noise decreases as expected due to the 1/f factor in 1/f noise formula.

The equation for thermal and 1/f noise are given below:

$$Thermal\ noise: 4kTR$$
$$\frac{1}{f} noise: \frac{K}{c_{ox} WL} * \frac{1}{f}$$

To reduce the 1/f noise, W*L product can be increased, frequency can be increased. Also for the thermal noise, R can be reduced to decrease noise of the amplifier.

Device	Param	Noise Contribution	% Of Total
/M0/m1	fn	4.30903e-07	62.77
/M3/m1	fn	4.00738e-08	5.84
/M20/m1	fn	6.77014e-10	0.10

Spot Noise Summary (in V^2/Hz) at 1K Hz Sorted By Noise Contributors
Total Summarized Noise = 6.86472e-07
Total Input Referred Noise = 1.30567e-12
The above noise summary info is for noise data

Fig. 11: Noise Analysis

As learnt in the class, in noise analysis, the uppermost and lowermost transistors have significant effects, the transistors in the bottom have negligible contribution for the noise. Looking at Fig. 11, M0 nMOS and M3 pMOS transistors have large contribution compared to M1 and M2 transistors. The input referred noise at 1KHz is measured as 1.3pV**2/HZ.

The total width of the whole amplifier design is 64µm. To adjust W of transistors, only number of fingers are changed for each transistor (2µm transistors are used).

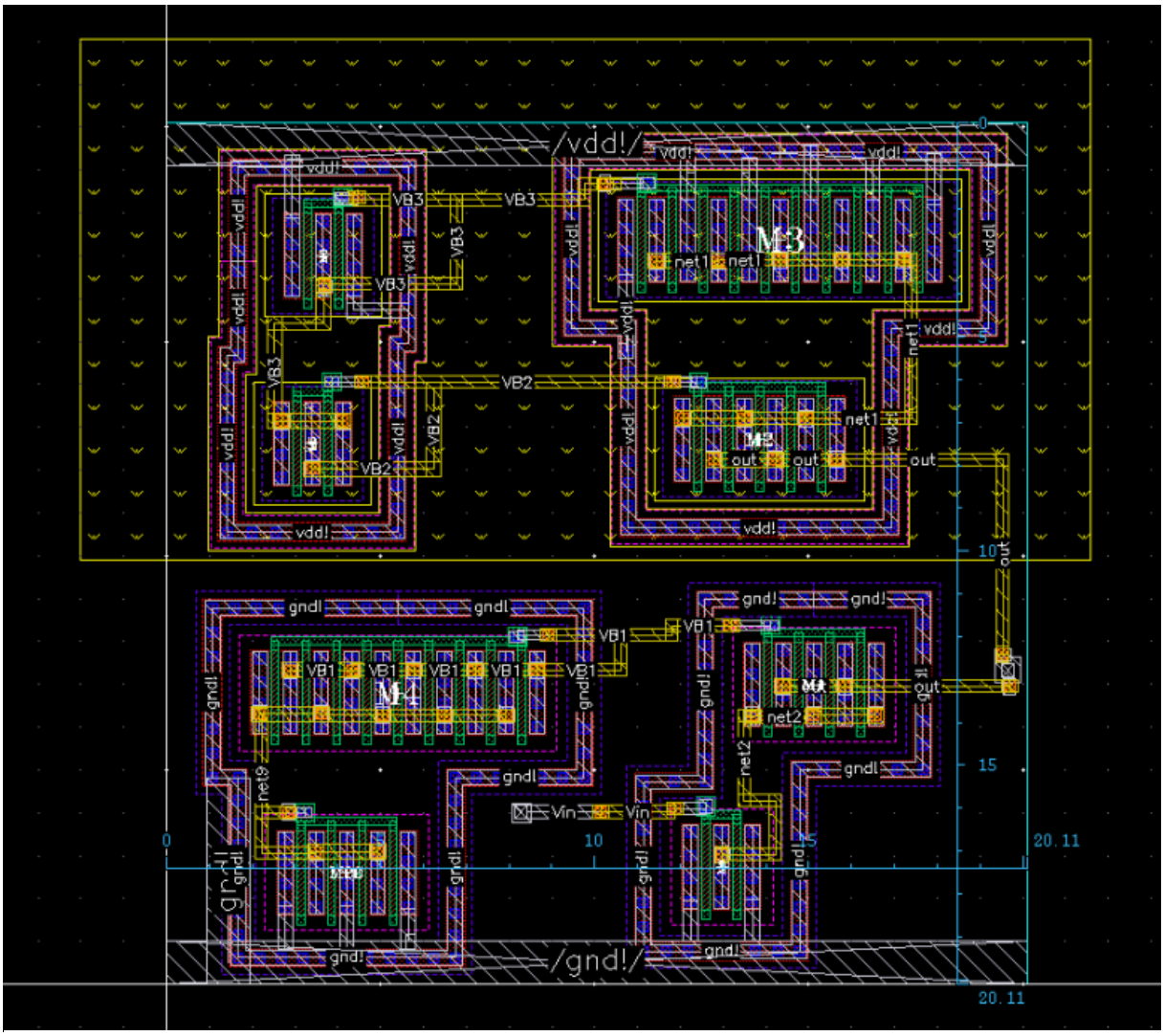


Fig. 12: Layout of the amplifier

The layout is created inside a 20µm x 20µm square. Upper half contains pMOS transistors and lower half contains nMOS transistors.

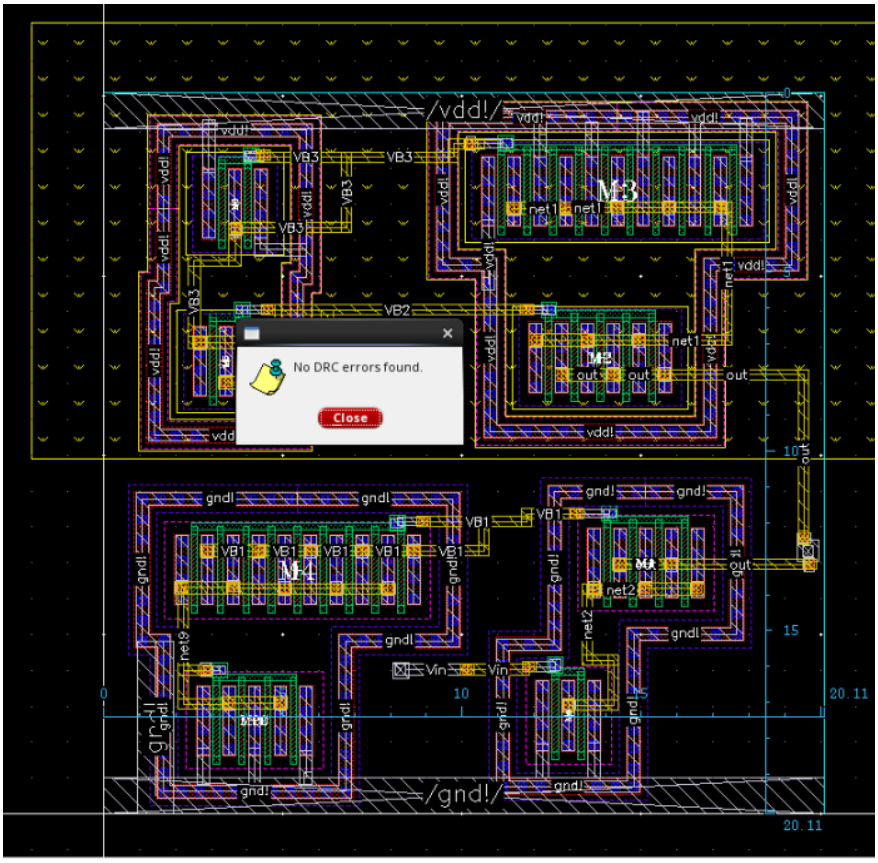


Fig. 13: DRC error-free

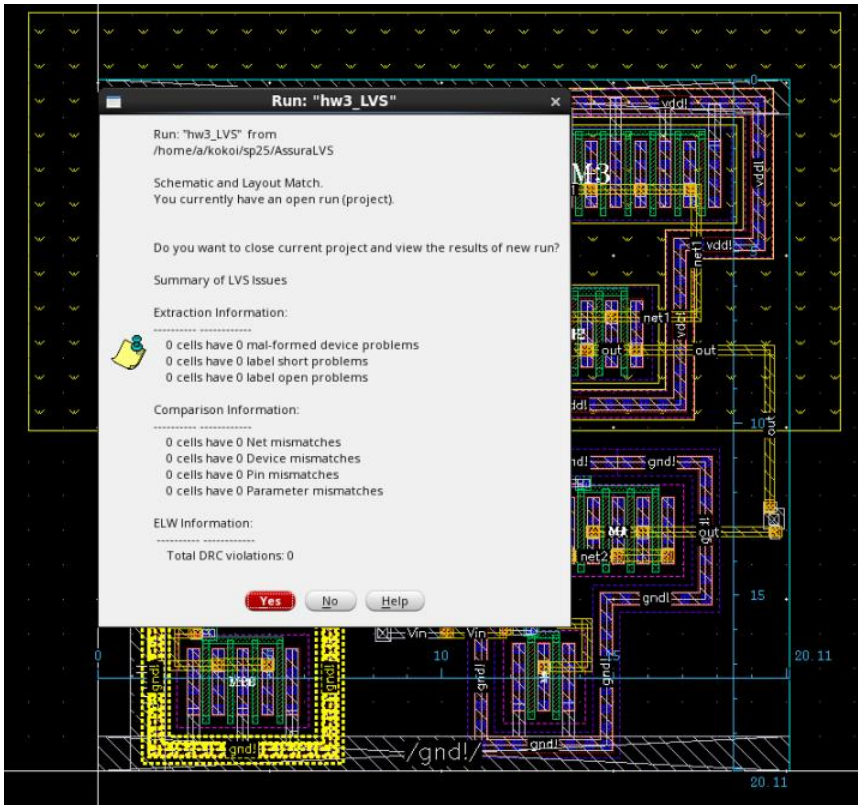


Fig. 14: LVS error-free