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Course Code: EEE313

Section: 02

Experiment Number: 02

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Lab 2 Preliminary Report

Introduction:

The experiment consists of two parts. First part (Part A) is about measuring β of a pnp transistor. For second part (Part B), the goal is to design a “Low-Dropout Voltage Regulator (LDO)”. LDO means the voltage difference between input voltage and output voltage is 0.7V maximum. Design specifications are listed below.

1. Line regulation: When Vin is between V_{out}+0.7 to V_{out}+6, the output voltage, Vout, changes by no more than 10mV when the output current is 20mA (R_L=Vout/0.02).

2. Load regulation: When Vin=Vout+2, the output voltage, Vout, changes no more than 50mV when the output current changes between 5mA and 100mA (R_L is varied between V_{out}/0.005 to V_{out}/0.1)

3. An output short circuit current of smaller than 250mA when V_{in}=V_{out}+0.7.

4. A green LED should turn on if the regulaƟon is achieved. Otherwise, it should turn off, for example, because the input voltage is too low or the output current is too high.

Methodology:

For Part A, I designed a simple pnp transistor circuit to measure β value for BD136 transistor. I will use (Eqn. 1) to find the β value of the pnp transistor. Circuit schematic can be seen below.

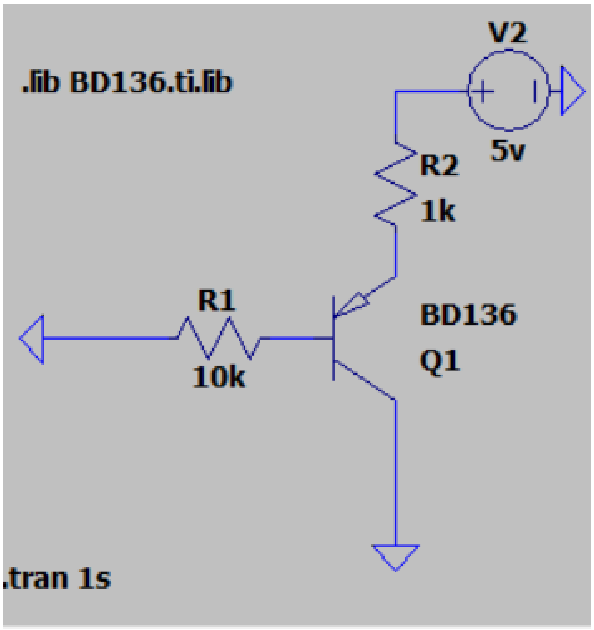

Figure 1: Part A schematic

For Part B, in order to design a LDO, I used two compatator OPAMPs and one BD136 pnp transistor, and one 6.8V zener diode. The purpose of using zener diode is to get constant voltage going into the comparator OPAMPs inverting (-) input. Regarding the voltage value at inverting input, I adjusted the output voltage that I chose to match with the zener diode breakdown voltage using a voltage divider at the non-inverting (+) input of the comparator OPAMP. The feedback capacitor connected to first comparator OPAMP is adjusting the value of voltage value changing no more than 10mV. The second comparator OPAMP is controlling the LED when to turn off and on. If the regulator is working properly, LED will turn on and otherwise, it will turn off. In order to make zener diode dissipate power less than 100mW, I connected a resistor to it in order to decrease the power consumption. The circuit schematic for Part B can be seen in the below figure.

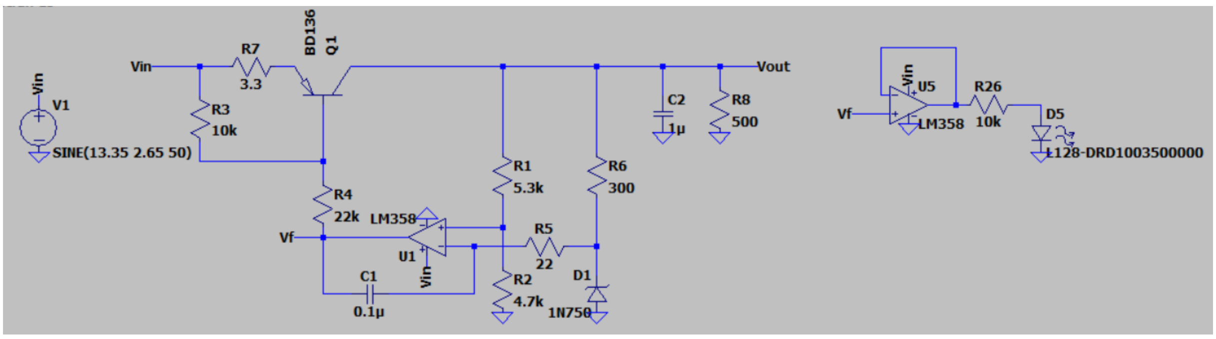

Figure 2: Part B schematic

Analysis:

Part A

$$I_C = \beta I_B$$

$$I_E = I_C + I_B = (\beta + 1) I_B$$

$$\beta = \frac{I_E}{I_B} - 1 \qquad \text{(Eqn. 1)}$$

(Eqn. 1) shows the relation of pnp transistor currents between each other. This equation is going to be used for finding the β value.

The figure below shows the base current (I_B).

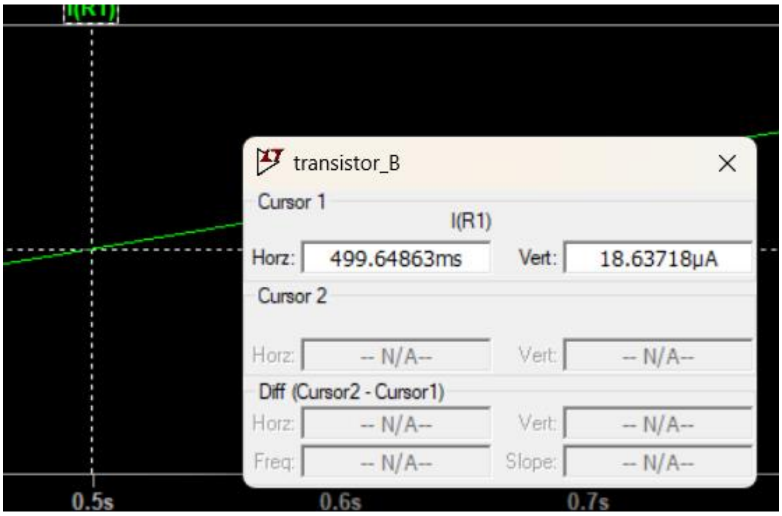

Figure 3: Base current

Now, the emitter current can be seen in the figure below.

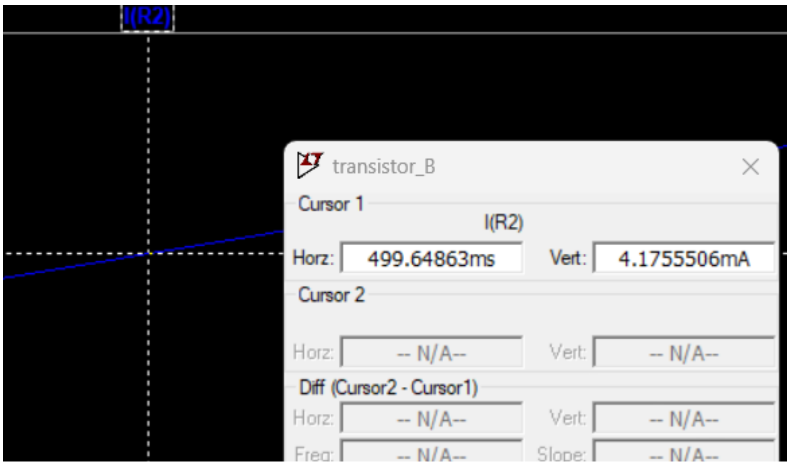

Figure 4: Emitter current

$$I_B = 18.64\mu A$$

$$I_E = 4.18mA$$

Inserting these values into (Eqn. 1), we get the following value for β:

$$\beta = 223.2$$

Part B

I chose my output voltage value to be 10V. Throughout the experiment, I did my calculations according to this value. First, I choose a zener diode with a 4.7V breakdown voltage. Then, using a voltage divider, I tried to get 4.7V from 10V. The reason for doing this is to get equal voltage values in the input of the comparator OPAMP. Therefore I choose my R1 and R2 to 5.3K and 4.7K respectively. I connected R6 in series with zener diode to limit the power consumption of the zener diode. Figure below shows how much power zener diode does consume.

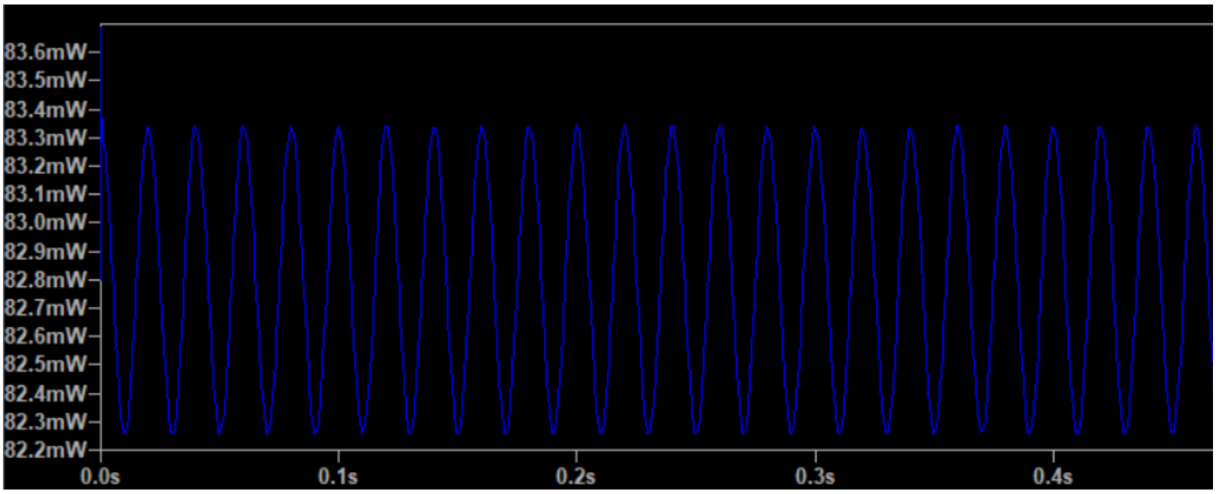

Figure 5: Zener diode power consumption

As seen, zener diode dissipates power less than 100mW.

In order to provide first specification, which is line regulation, I played with the capacitor value connected to the first OPAMP as a feedback element and the resistor connected series to it. By playing with their values, I am able to change the band of frequency. Therefore I get maximum of 10mV change at the V_{out}. The difference at the output when V_{in} varies between V_{out} + 0.7V = 10V and V_{out} + 6V = 16V can be see in the figure below.

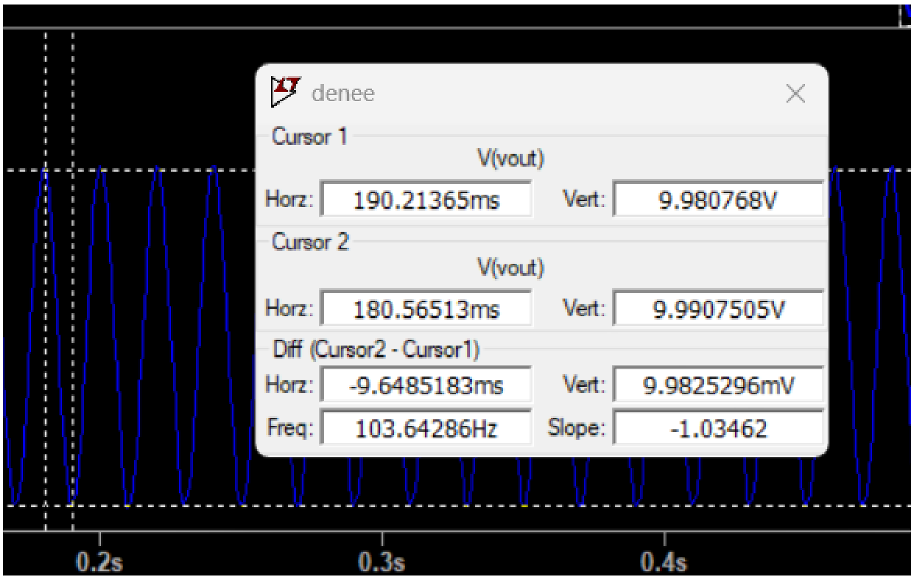

Figure 6: 9.98mV difference at output

The current at the load (R_L=500Ω) is given in the figure below.

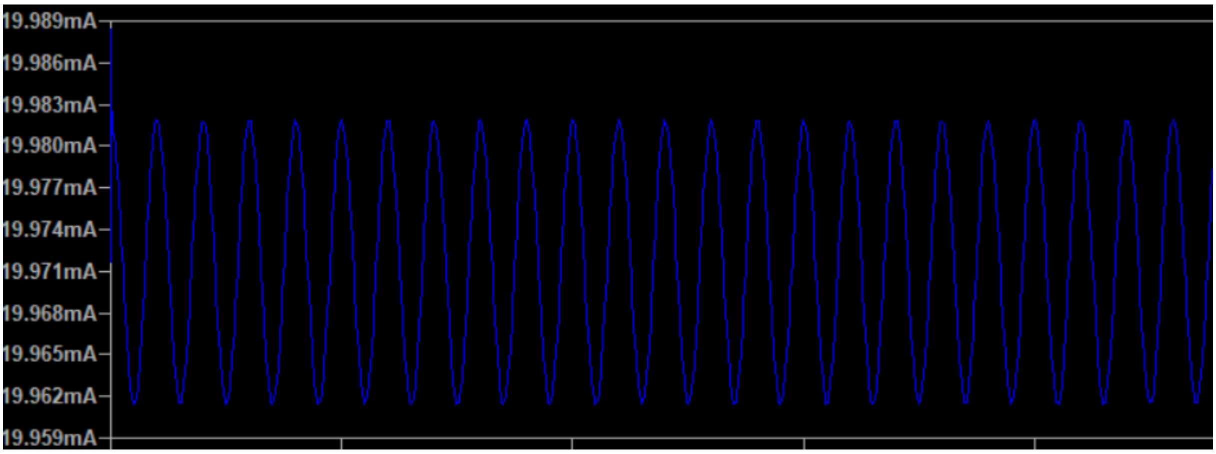

Figure 7: Current at load resistance (R_L=500Ω)

For the second specification, which is load regulation, it is wanted that when $V_{in} = V_{out} + 2V = 12V$, V_{out} changes no more than 50mV when the output current changes between 5mA (R_L = 2000 Ω) and 100mA (R_L = 100 Ω).

Figure 8 shows the current value when R_L = 2000 Ω.

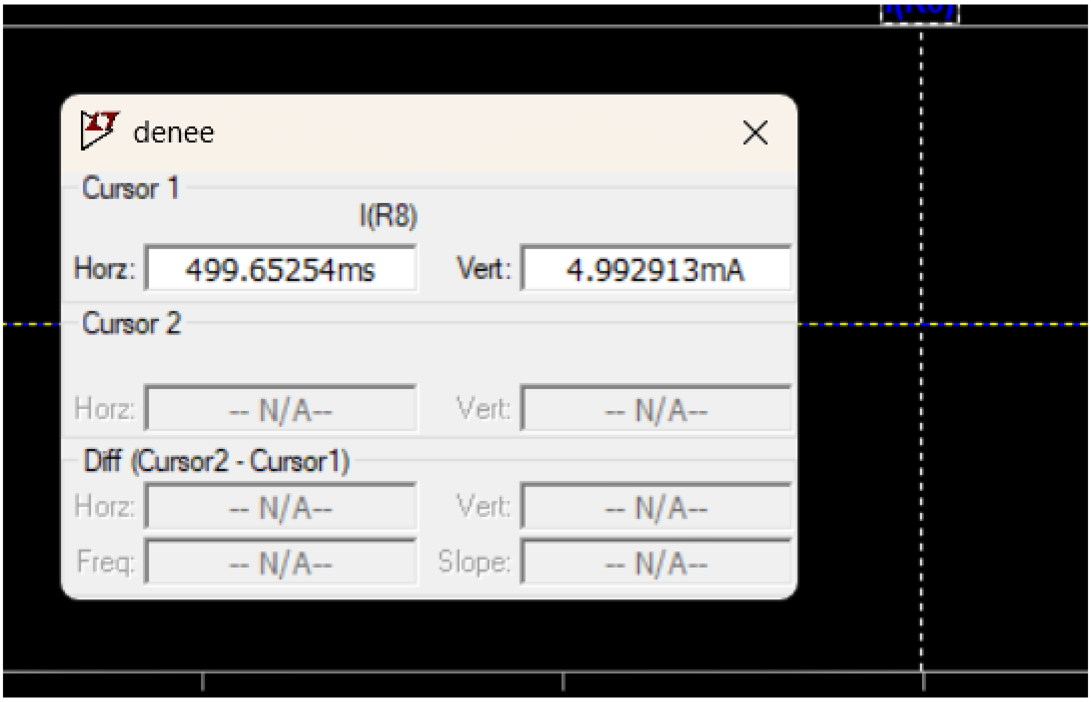

Figure 8: Current at R_L = 2000 Ω

Figure 9 shows the current value for R_L = 100 Ω.

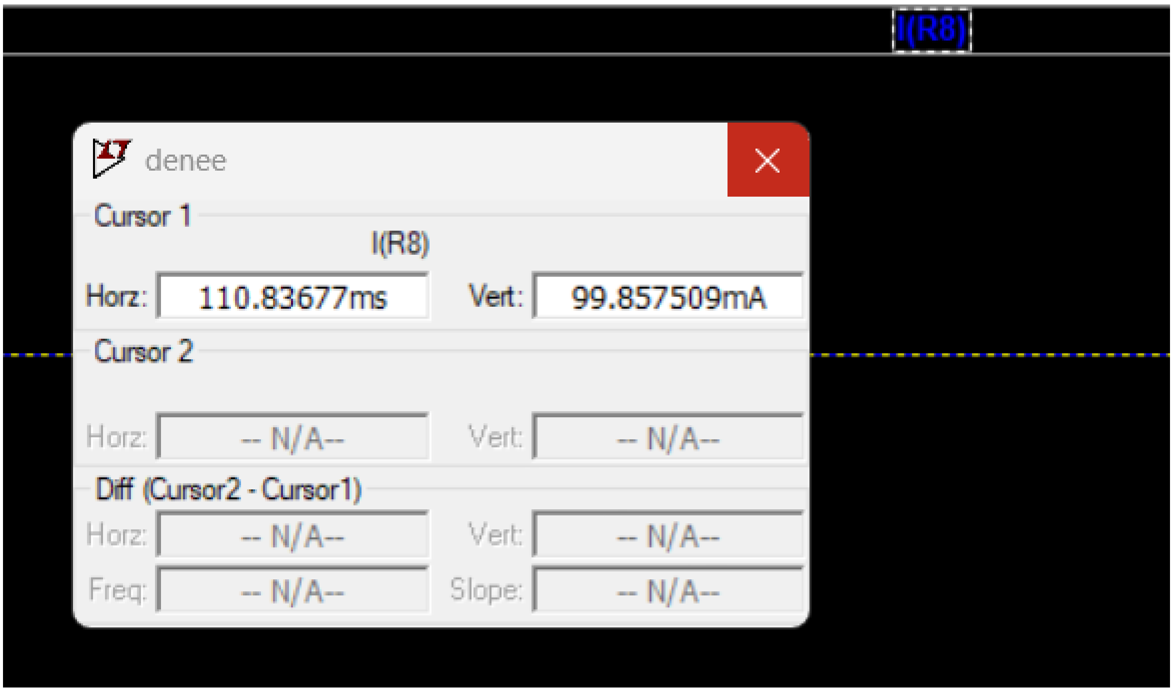

Figure 9: Current at R_L = 100 Ω

The figures below (Figure 10 and Figure 11) shows the voltage values when R_L = 2000 Ω and R_L = 100 Ω relatively.

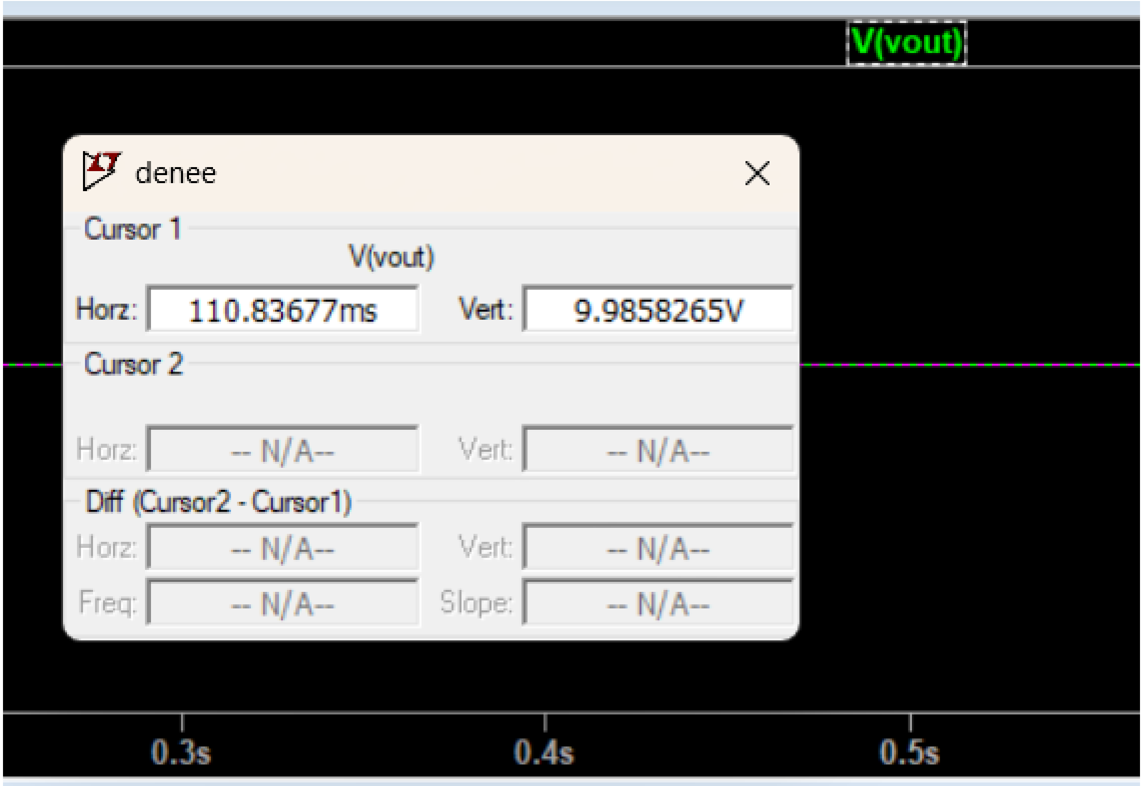

Figure 10: Output voltage at R_L = 2000 Ω

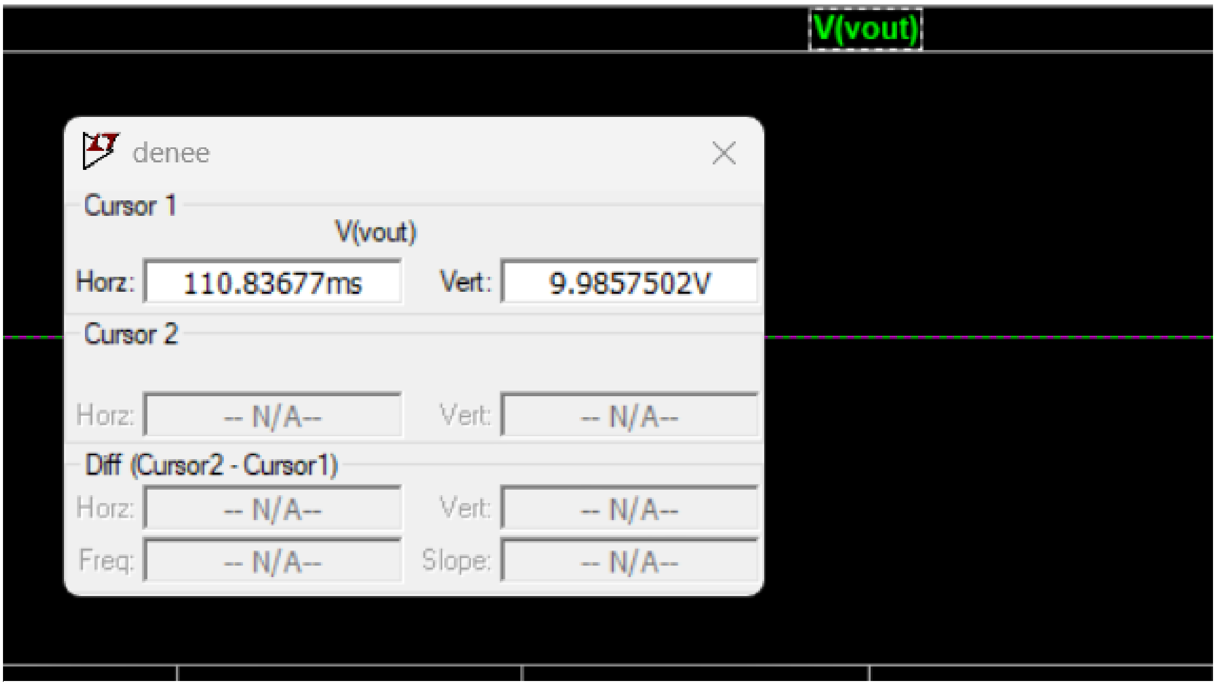

Figure 11: Output voltage at R_L = 100 Ω

As seen from Figure 10 and Figure 11, voltage difference when R_L changes from 100Ω to 2000Ω is less than 50mV. The difference is 0.07mV.

Table 1: Current and Voltage value comparison for variable load resistance

	R_L = 2000 Ω	R_L = 100 Ω
Current Value	99.87mA	4.99mA
Output Voltage Value	9.9858V	9.9857V

For the third design specification, it is wanted that when $V_{in} = V_{out} + 0.7V$, output short circuit current should be less than 250mA. To measure the output short circuit current, I changed the load resistance value to R_L=1Ω. Below figure shows the output short circuit current value.

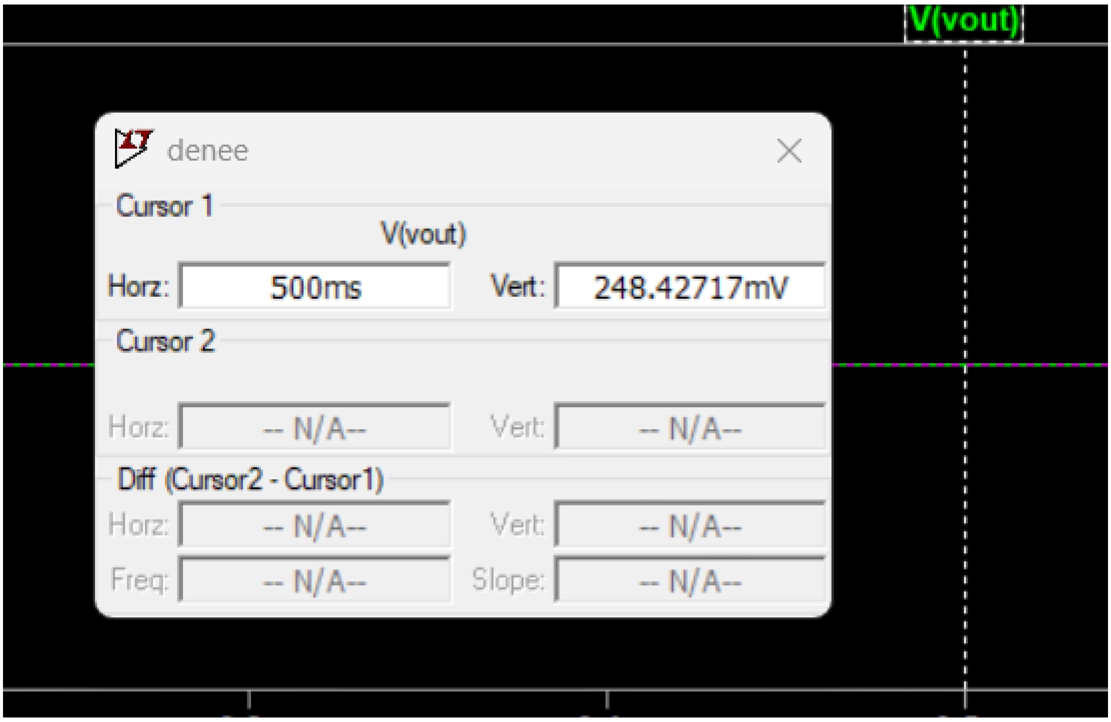

Figure 12: Output short circuit current

The last specification is turning an LED on when the regulation is perfomed correctly. In order to do it, I used a second OPAMP. The non-inverting output is the output of the first OPAMP. By that, when regulation cannot perfomed correctly, output of the first OPAMP will be close to 0V, and comparing it with itself will give us 0V. Therefore I connected inverting input directly to the output. So, whatever the input value is, output value will be the same. So, whenever output of the first comparator OPAMP (LDO OPAMP) is greater than zero, LED will turn on. Otherwise, because LDO cannot work properly maybe input voltage is to low, LED will turn off.

For instance, when I give 10.7V as V_{in}, Figure 13 shows that there is current passing through LED which means it turns on.

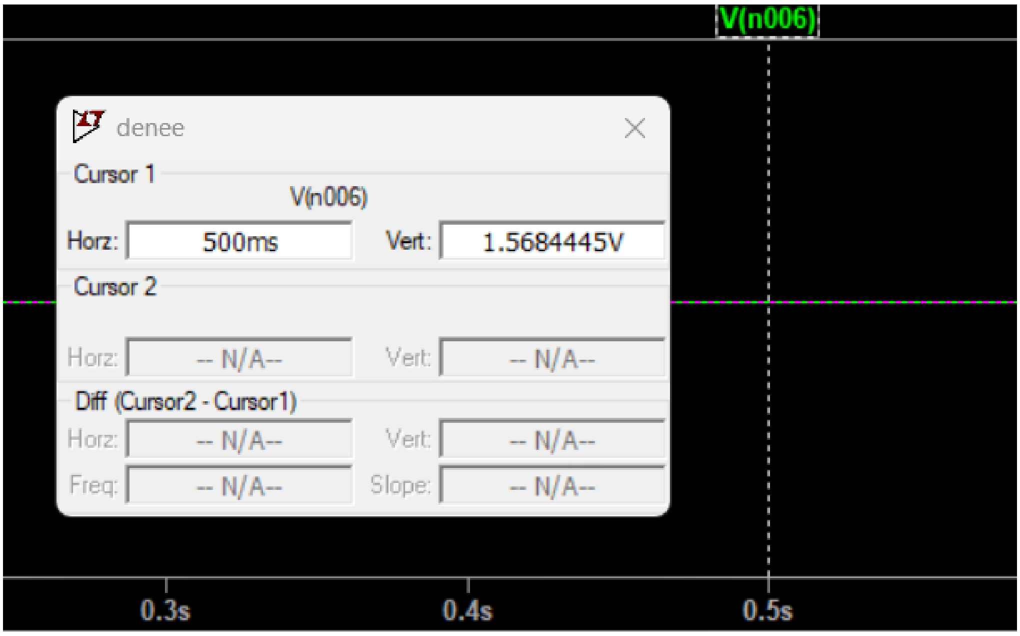

Figure 13: LED voltage when V_{in} = 10.7V

When I decrease the V_{in} to 9.5V, LED will turn off due to improper regulation. Figure 14 shows the output voltage of the LDO and Figure 15 shows the LED voltage accordingly when V_{in} = 9.5V.

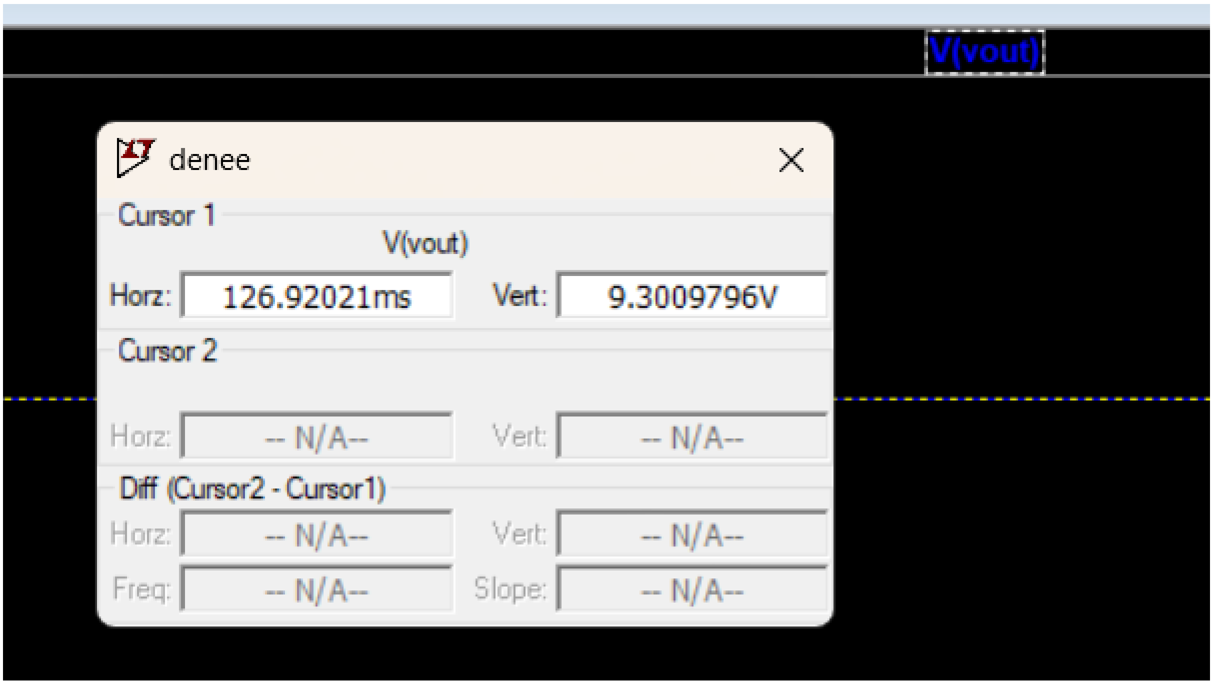

Figure 14: Output voltage of LDO when V_{in} = 9.5V

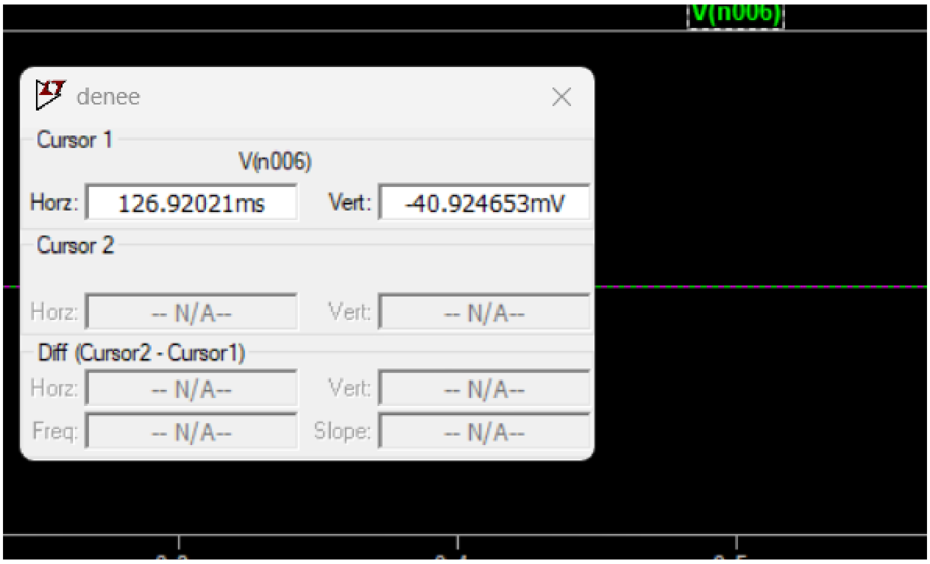

Figure 15: Voltage across the LED when V_{in} = 9.5V

To meet the "Thermal Analysis" requirement, looking at the datasheet of BD136 transistor, I found the junction to ambient thermal resistance ($R_{\theta JA}$), juncΘon to case thermal resistance ($R_{\theta JC}$), and the maximum juncΘon temperature (T_{Jmax}).

$$R_{\theta JC} = 10°C/W$$

$$R_{\theta JA} = 100°C/W$$

$$T_{Jmax} = 150°C$$

Using these values, junction temperature (T_J) value will be calculated. Calculations are going to be made at 25$°C$, when $V_{in} = V_{out} + 3V = 13V$, and $R_L = 90\Omega$ (drawing 80mA of current).

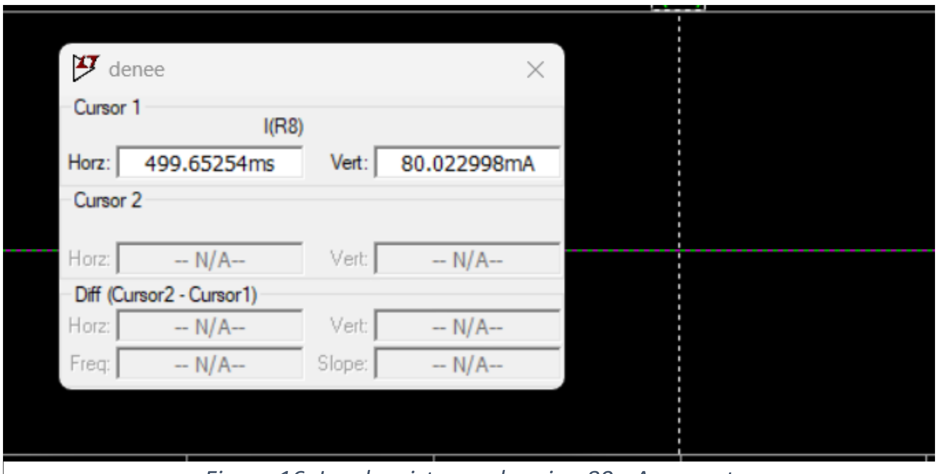

Figure 16: Load resistance drawing 80mA current

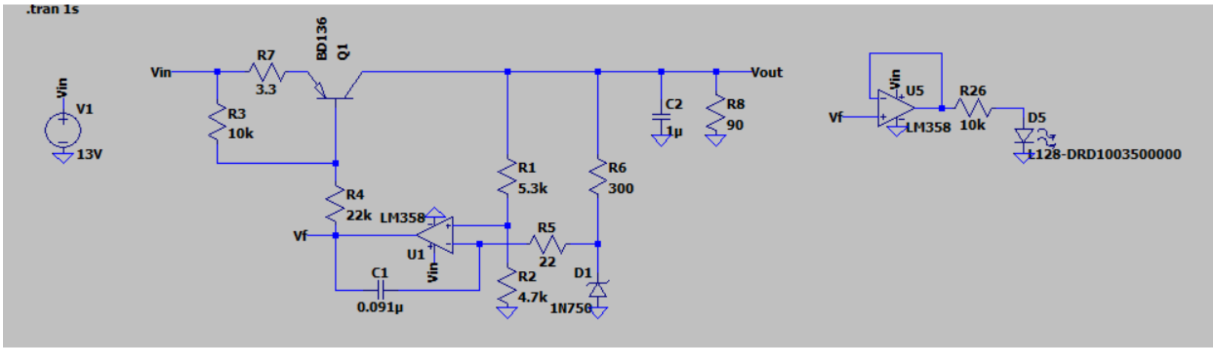

Figure 17: Thermal Analysis Circuit Schematic

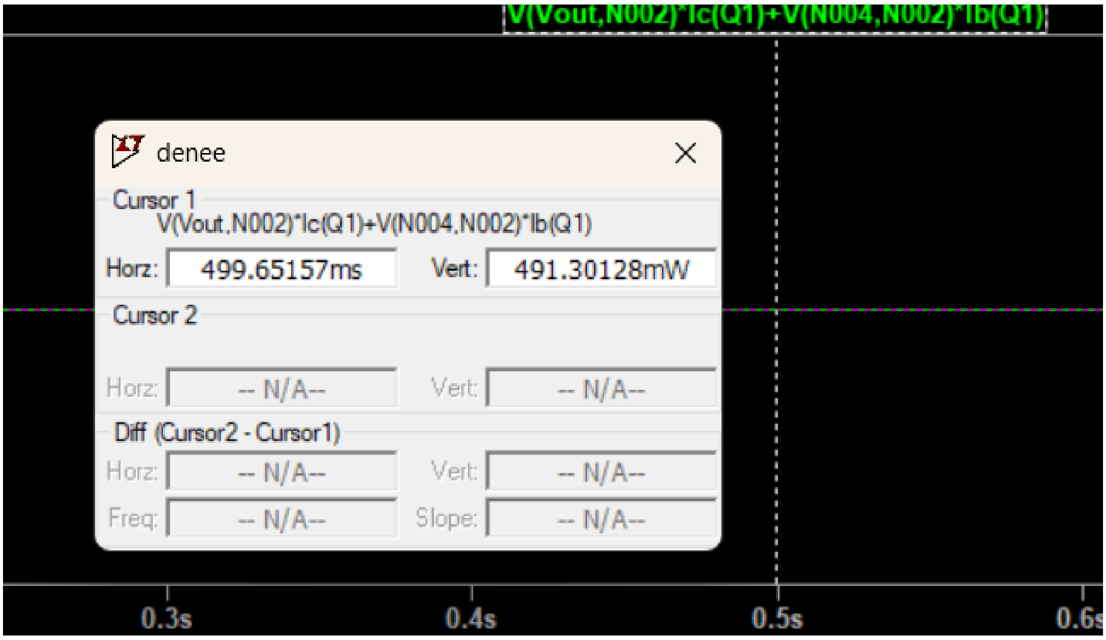

Figure 18: Transistor's power dissipation

$$T_J - T_A = R_{\theta JA} * P_D; \qquad \textit{where } P_D \textit{ is transistors power dissipation} \qquad \text{(Eqn. 2)}$$

From found and measured values, junction temperature calculated as $T_J = 49.75°C$.

Now, from (Eqn. 3), case temperature (T_C) value can be calculated.

$$T_J - T_C = R_{\theta JC} * P_D \qquad \text{(Eqn. 3)}$$

$$T_C = 44.84°C$$

Figure below shows the DipTrace circuit schematic of LDO voltage regulator (Part B).

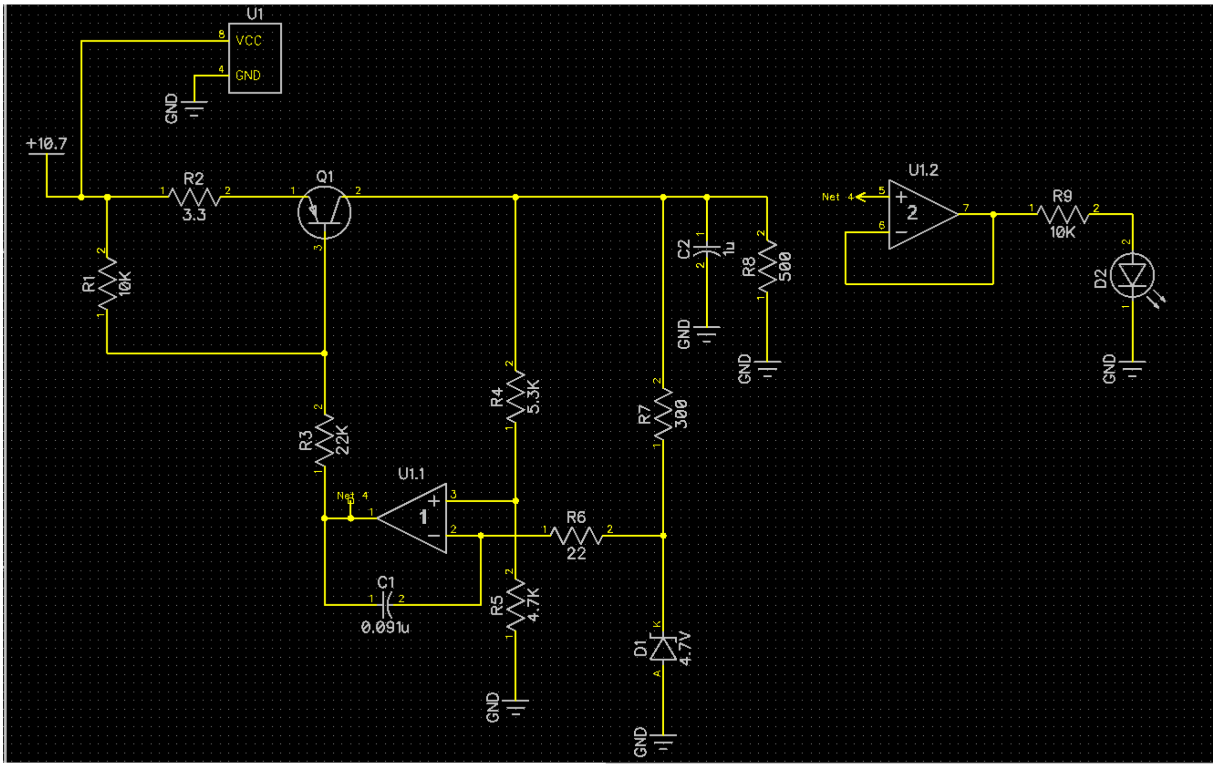

Figure 19: DipTrace schematic of the design

Figure 20 shows the used material table for the desgined LDO voltage regulator schematic.

#	RefDes	Value	Name	Quantity
1	C1	0.091u	CAP100	1
2	C2	1u	CAP200	1
3	D1	4.7V	DIO_ZENER	1
4	D2		LED	1
5	Q1		BD136G	1
6	R1, R9	10K	CFR-25JB-52-1K	2
7	R2	3.3	CFR-25JR-52-10K	1
8	R3	22K	CFR-12JB-52-10K	1
9	R4	5.3K	CFR-12JB-52-100K	1
10	R5	4.7K	CFR-50JB-52-100K	1
11	R6	22	CFR100JR-52-100K	1
12	R7	300	CFR200JR-73-10K	1
13	R8	500	CFR25SJR-52-100K	1
14	U1		LM358N	1

Figure 20: Material list for designed circuit