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Course Code: EEE313

Section: 02

Experiment Number: 03

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Lab 3 Preliminary Report

Introduction

The purpose of this experiment is designing a complementaru push pull Class-B amplifier. The amplifier should deliver at least 2.25W to the 8.2Ω load resistor. The supply voltages are chosen as ±9V. Design specifications are listed below:

1. The amplifier should deliver at least a 2.19W power to an 8.2Ω resistance (12Vpp to an 8.2Ω power resistor) starting from 10Hz to 40KHz at the chosen gain value.

2. The harmonics (the highest is possibly the third harmonic) at the 2.25W output power level should be at least 40 dB lower than the fundamental signal at 1 KHz.

3. The power consumption at quiescent conditions should be less than 500mW.

4. The amplifier's overall efficiency (output power/total supply power) should be at least 45% at max power output at 1KHz.

Methodology

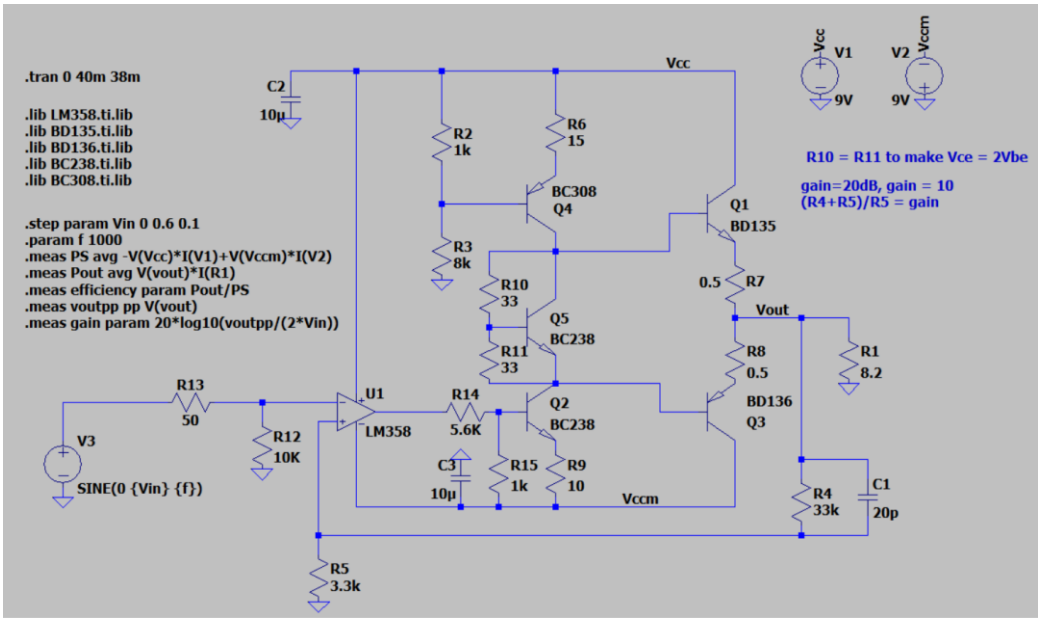

Figure 1: Circuit Schematic

As shown in the figure above (Figure 1), R4 and R5 resistor values are chosen as 33.3KΩ and 3.3KΩ. These values are chosen to obtain 20dB gain between output and input, (Eqn. 1) shows the gain relation.

$$V_{out} = \frac{R4+R5}{R5} V_{in} \qquad \text{(Eqn. 1)}$$

$$20 \log_{10}(gain) = dB\ gain$$

When input chose the input voltage starting from 0 to 0.6V, Figure 2 shows the output voltage magnitude values. As expected, 20dB gain is obtained. (From 0.6V to 6V).

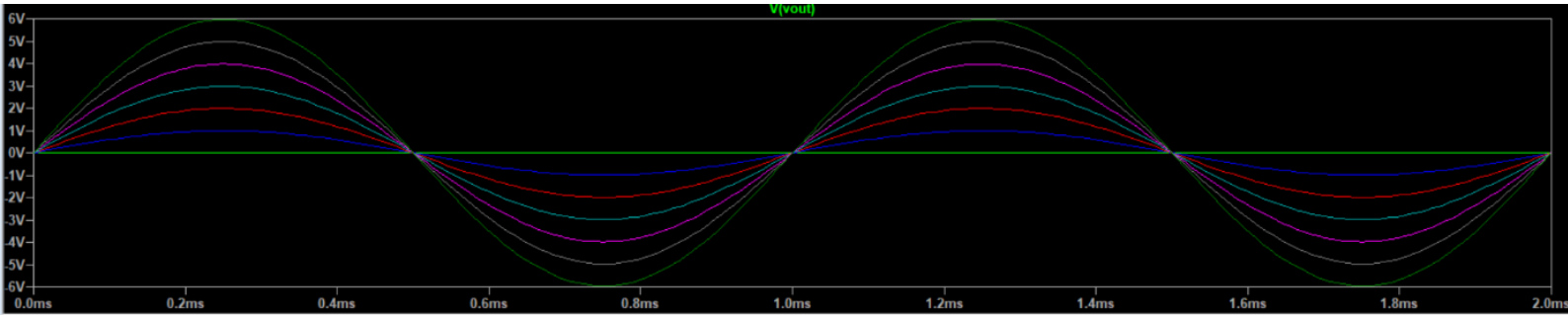

Figure 2: Output Voltage

To create a current source with a value between 15-20mA using the BC308 pnp transistor, I did a series of calculation to determine the values of resistors R2 and R3. To determine resistor equations, I assumed V_{EB}=0.7V. From this point, I found V_B as 8.075V. Also choosing the R2 value as 1KΩ. Using (Eqn. 2), R3 value is calculated.

$$\frac{V_B}{R3} = I_B + \frac{9-V_B}{R2} \qquad \text{(Eqn. 2)}$$

From (Eqn. 2), R3 value is calculated as 868Ω. I choose the closest standard resistor values which is 8KΩ. Figure 3 shows the current value of the created current source.

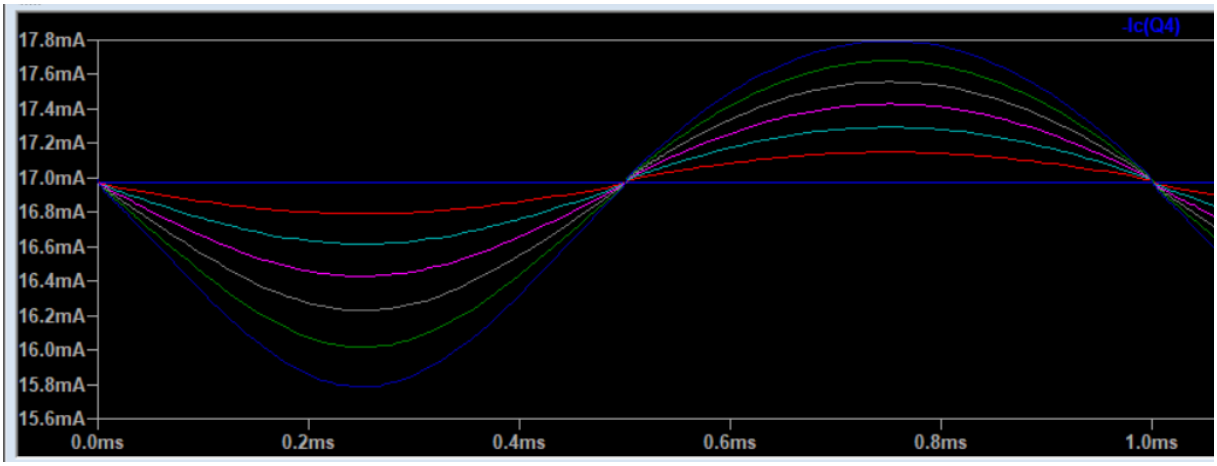

Figure 3: Current source with a value of 17.75mA

C1 capacitor value is chosen by trial and error as 10pF. The effect of this capacitor is preventing the potential oscillations that may occur at the output voltage.

For the V_{BE} multiplier, it is wanted that $V_{CE}=2V_{BE}$. To provide this equality, R10 and R11 resistor values are chosen as same with each other. They are chosen as 33Ω. Because at ths value, emitter currents of Q1 and Q3 become high and acts complementary (Figure 4).

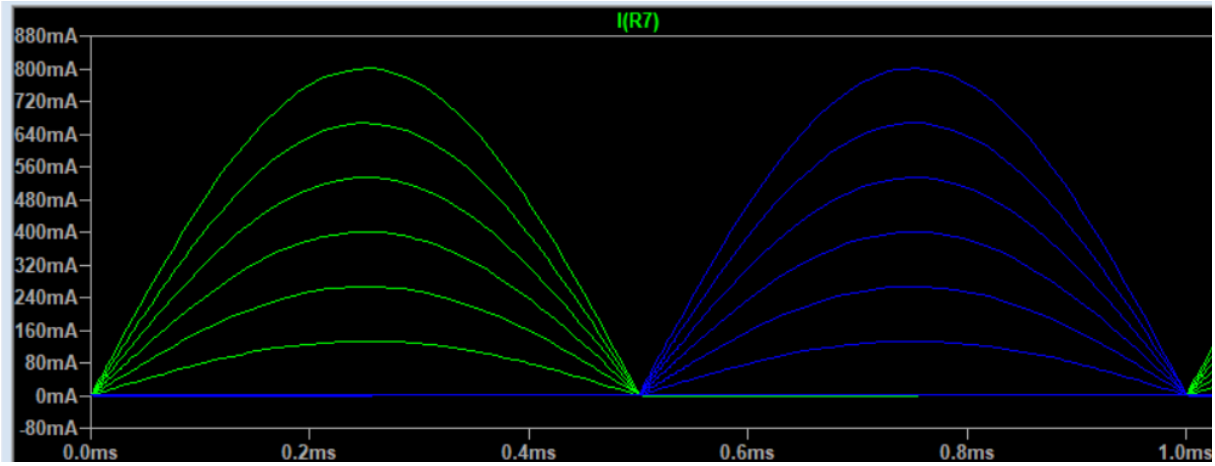

Figure 4: Emitter currents of Q1 and Q3

Analysis

First specification:

I choose my input voltage as 0.6V AC with variable frequency values starting from 10Hz to 40KHz. The following figure shows the power delivered to load resistor.

Measurement: pout

step	AVG(v(vout)*i(r1))	FROM	TO
1	2.62353	0	0.002
2	2.59118	0	0.002
3	2.57471	0	0.002
4	2.54256	0	0.002
5	2.50118	0	0.002

Figure 5: Power delivered to load starting from 10Hz to 40kHz

The design specification wants at least 2.19W should be delivered to load. The power delivered at load varies between 2.62W to 2.5W.

Second Specification:

For this part, harmonic at 3KHz should be at least 40dB lower than the harmonic at 1KHz. Figure below shows the dB difference between these two harmonics. V_{in} is 0.6V throughout the measurements to obtain 2.25W at the load.

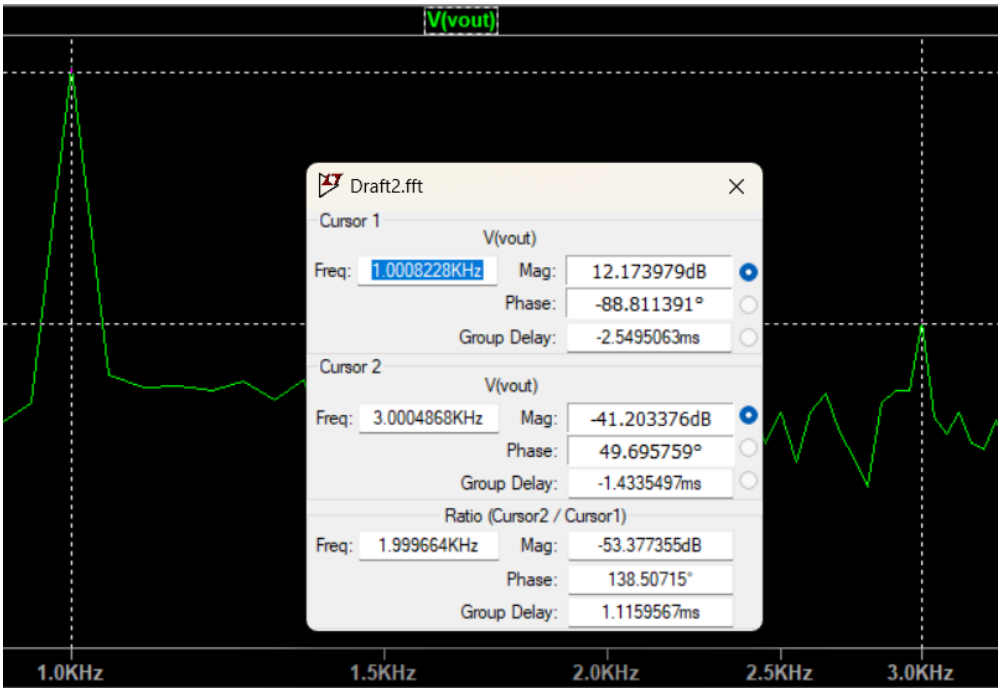

Figure 6: Harmonics at 1KHz and 3KHz

As seen from the Figure 6, fundamental harmonic (1KHz) is at 12.17dB, and third harmonic (3KHz) is at -41.20dB. Looking at the difference between these two harmonics, it can be said that third harmonic is 53.38dB lower than the fundamental harmonic, which is greater than 40dB. Therefore second specification is satisfied.

Third Specification:

To measure power dissipation at quiescent condition, I observed the power at load when the input voltage is 0V. I changed the load resistance value to 1Ω. Figure 7 shows the results.

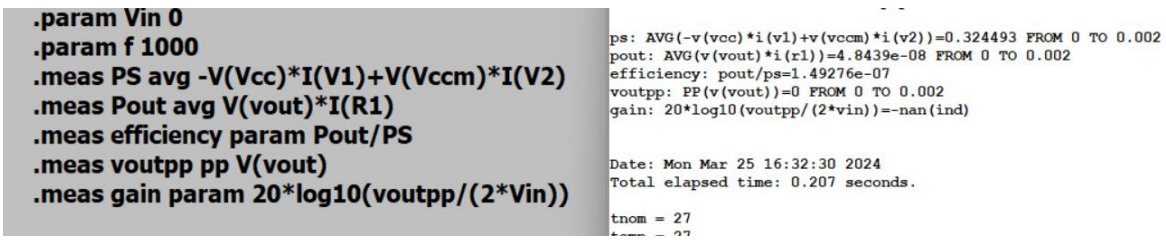

Figure 7: Power consumption at quiescent condition at load

As seen in Figure 7, when V_{in}=0V, power consumption (ps) is 324mW, which is below 500mW. Therefore third specifications is also satisfied.

Fourth Specification:

This specification wants the efficiency of the circuit should be at least 45% at max power output when frequency is 1KHz.

```
.step param Vin 0 0.6 0.1
.param f 1000
.meas PS avg -V(Vcc)*I(V1)+V(Vccm)*I(V2)
.meas Pout avg V(vout)*I(R1)
.meas efficiency param Pout/PS
.meas voutpp pp V(vout)
.meas gain param 20*log10(voutpp/(2*Vin))
```

```
Measurement: efficiency
  step            pout/ps
     1            1.49276e-07
     2            0.0675725
     3            0.158863
     4            0.25315
     5            0.348435
     6            0.444283
     7            0.540598
```

Figure 8: Efficiency of the circuit

Looking at the 7th step in the table, when V_{in}=0.6V and frequency is at 1KHz, efficiency of the circuit is 54%, greater than 45%. Therefore, the last condition is also satisfied.

DipTrace schematic of the circuit can be seen in the figure below.

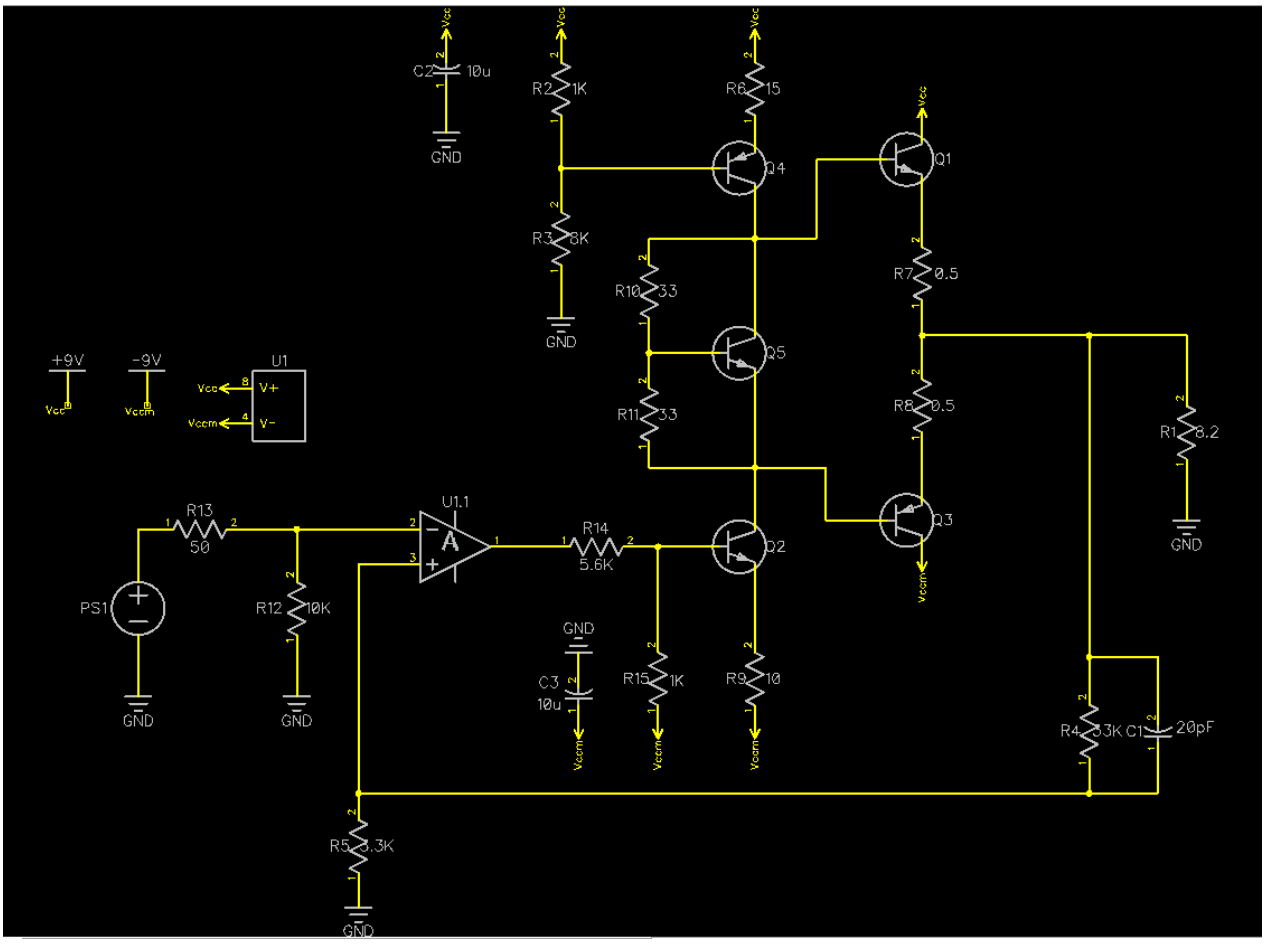

Figure 9: DipTrace Circuit Schematic

Bill of materials can also be observed in the figure below.

#	RefDes	Value	Name	Quantity
1	C1, C2, C3	20pF	CAP100	3
2	PS1		VOLTAGE_SINE	1
3	Q1		BD135G	1
4	Q2, Q5		BC238	2
5	Q3		BD136G	1
6	Q4		BC308	1
7	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15	8.2	CFR-12JB-52-100K	15
8	U1		LM358D	1

Figure 10: Bill of Materials