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Department: EEE

Course Code: EEE313

Section: 02

Experiment Number: 04

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Lab 4 Preliminary Report

Introduction

The purpose of this experiment is desinging a two-stage RC coupled amplifier with feedback. For amplification, BJT or MOS transistors will be used. Design specifications are given below.

Specifications:

- Source impedance: 500Ω
- Load impedance: 47Ω
- Voltage Gain: 20 dB±0.5dB
- Bandwidth (−3dB): at least 5KHz to 5MHz
- Supply voltage: 12V (single supply)
- Maximum current consumption: 70mA from the supply voltage
- Undistorted peak-to-peak output voltage: 2Vpp at 500KHz.
- Distortion at the output: Harmonics less than −30dBc at 500KHz 2Vpp output voltage (the difference between the fundamental and the highest harmonic in FFT window)

Methodology

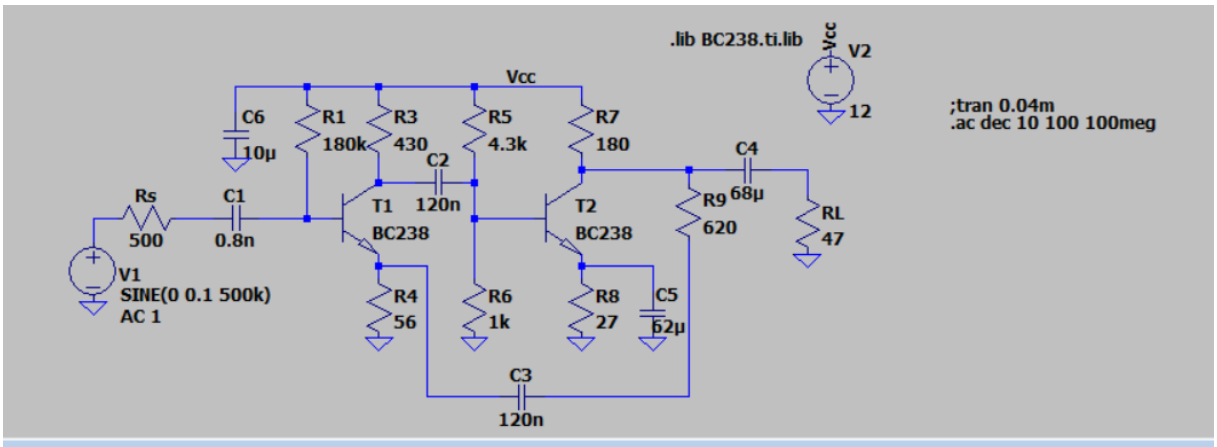

Fig. 1: Circuit Schematic

I used two BC238 BJT's in my design. I choose T_1 collector current as 15mA and T_2 collector current as 50mA. The sum is less than 70mA. To make voltage across R4 and R8 equals to 1V, calculations are made according to Eqn. 1.

$$V = \frac{I}{R}$$

$$R = \frac{1}{I_c} \qquad \text{(Eqn. 1)}$$

R4 value is calculated as 56Ω and R8 value is calculated as 27Ω. A small adjustment is done on R4 to obtain desired results.

For choosing value of R1 resistor, I solved the DC analysis of T1, assuming V_{BE} = 0.7V. From there, R1 = 137kΩ, I changed it to 180kΩ to make the current less than 70mA.

According to specifications, current across R5 is 1/20 of collector current of T2. I_{R5} = 2.5mA. Again performing DC analysis while assuming V_{BE} = 0.7V, R5 value is found as 4120Ω, I used 4.3kΩ in my design. I choose R6 value as 1kΩ to get 50mA as the collector current of the T2 transistor.

However, when I make R9/R4 ratio as 10, which is equal to 20dB, I get 20dB in small signal analysis, but in transient analysis, I get 1V pk-pk while the input is 0.1V pk-pk.

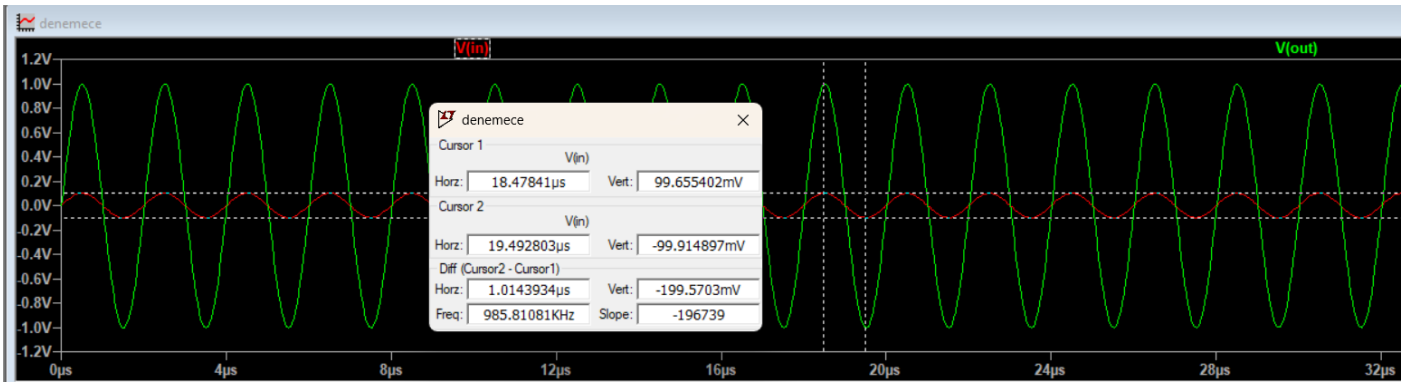

Fig. 2: Vout vs Vin at 500kHz

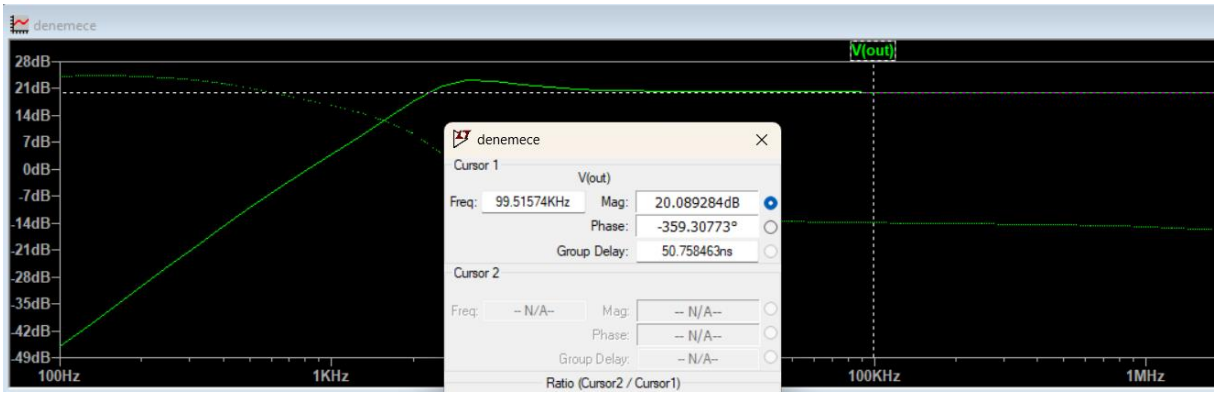

Fig. 3: 20dB gain at output

R9 value is still chosen as 620. R9/R4 = 11.

Eqn. 2 is the formula for DC-block capacitors.

$$f = \frac{1}{2\pi RC} \qquad \text{(Eqn. 2)}$$

Using this formula, below given the values of capacitors.

C1 = 0.8nF

C2 = 120nF

C3 = 120nF

C4 = 68µF

C5 = 62µF

C6 = 10µF

To get the maximum values for R3 and R7, I assumed V_{CE} = 0.2V and again performed DC analysis for both T1 and T2 transistors. After donig the calculation, R3 found as 430Ω and R7 found as 180Ω.

Analysis

First Specification:

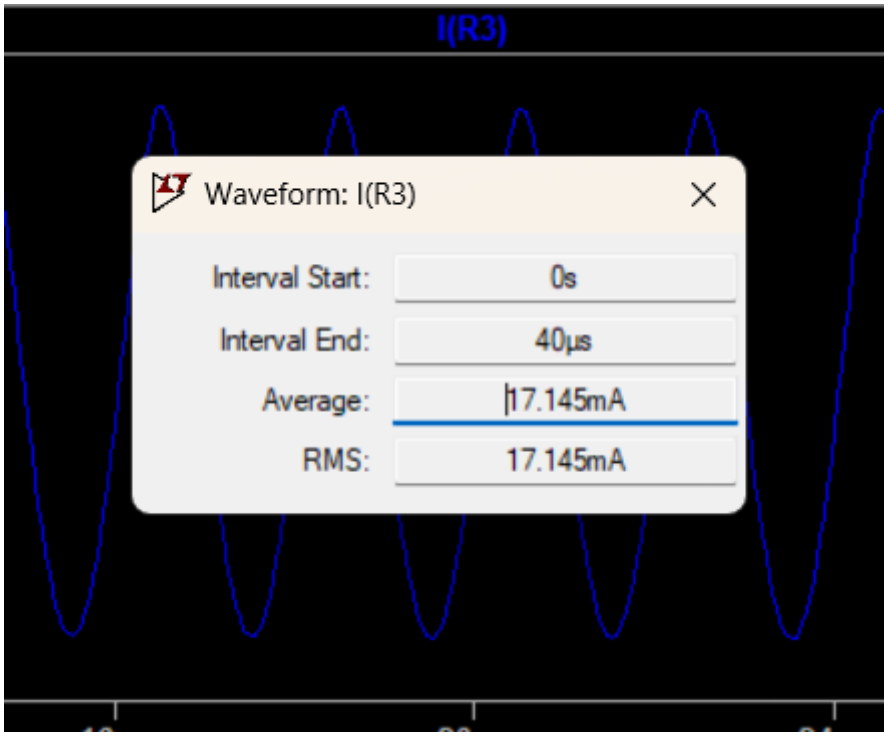

Fig. 4: Current of T1

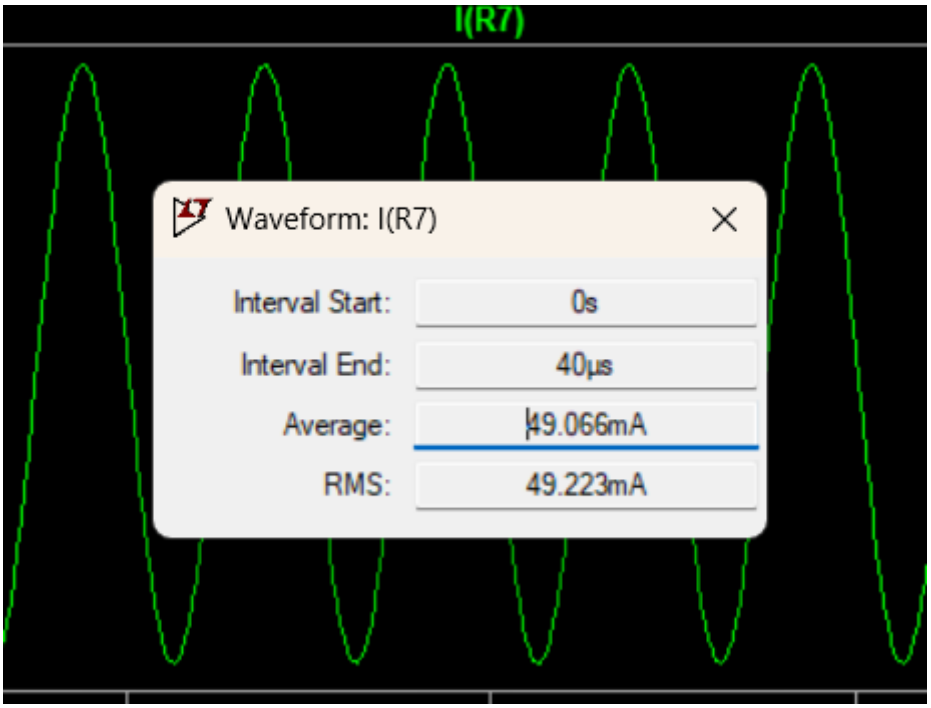

Fig. 5: Current of T2

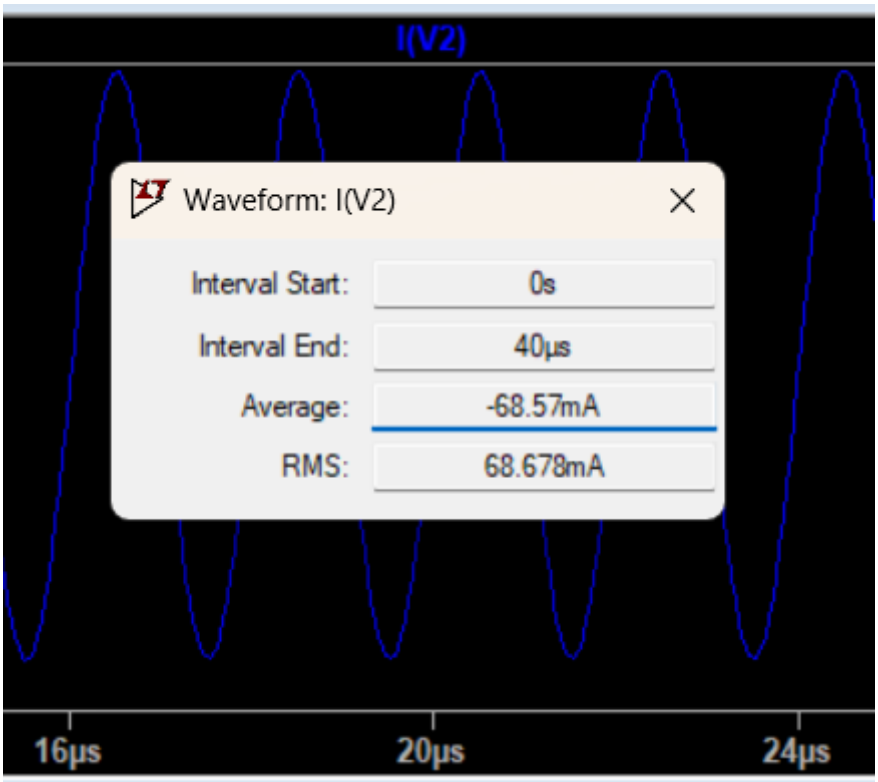

Fig. 6: Current consumption of the circuit

In methodology, collector current of T1 is chosen as 15mA, in analysis, it is measured as 17.1mA. Similarly, in methodology, collector current of T2 is chosen as 50mA, in analysis, it is measured as 49.1mA. Therefore, with a slight error included, desired results are obtained.

For the current consumption of the circuit, it is measured as 68.57mA, which is less than 70mA. So, first specification is satisfied.

Second Specification:

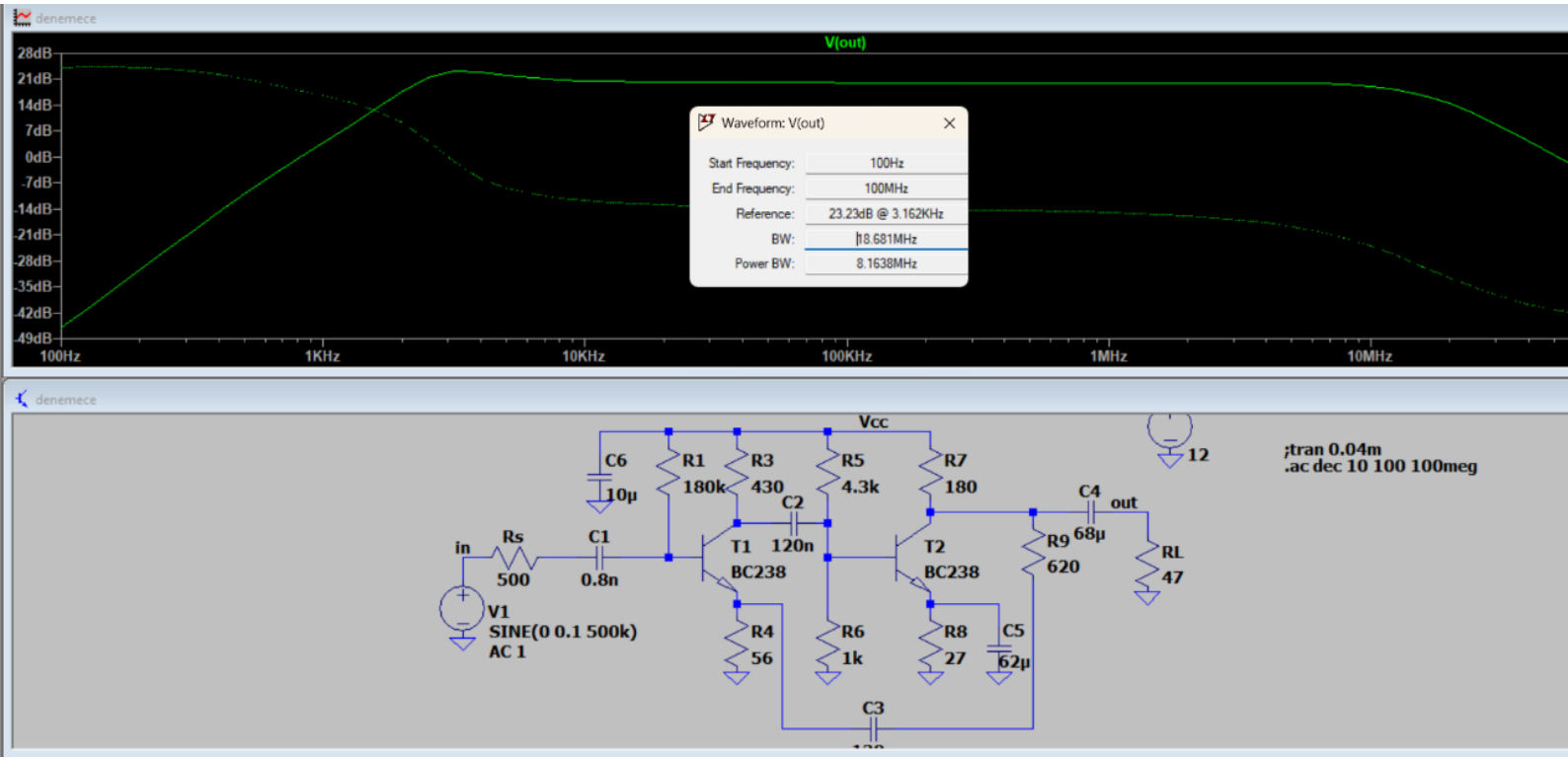

Fig. 7: BW of the designed circuit

Fig. 7 shows the bandwith of the the designed circuit. BW is measured as 18.68MHz. -3dB points are 700Hz and 61.5MHz.

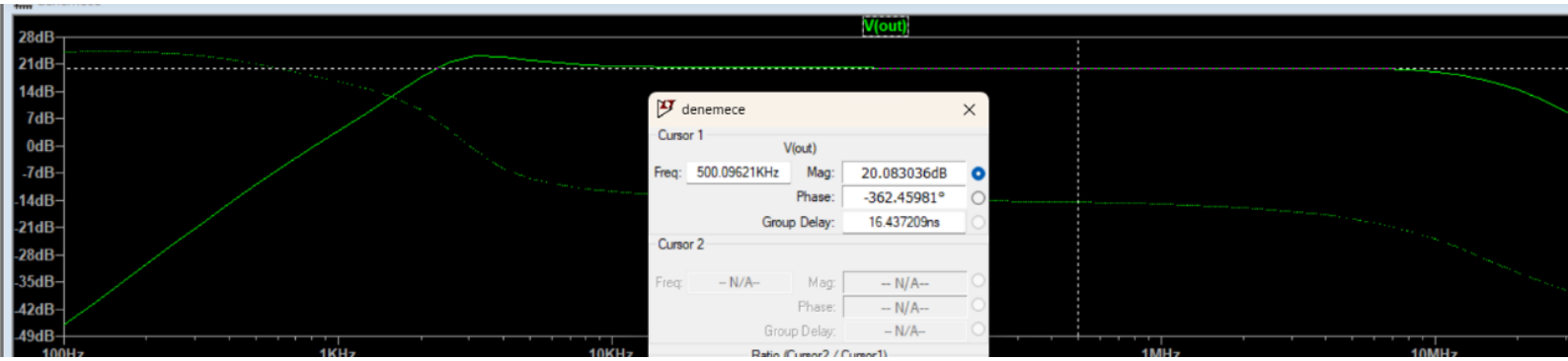

Fig. 8: dB gain at 500kHz

As seen from Fig. 8, at 500kHz, dB gain is 20.08, an gain is flat from 7kHz to 11MHz. Therefore second specification is also satisfied.

Third Specification:

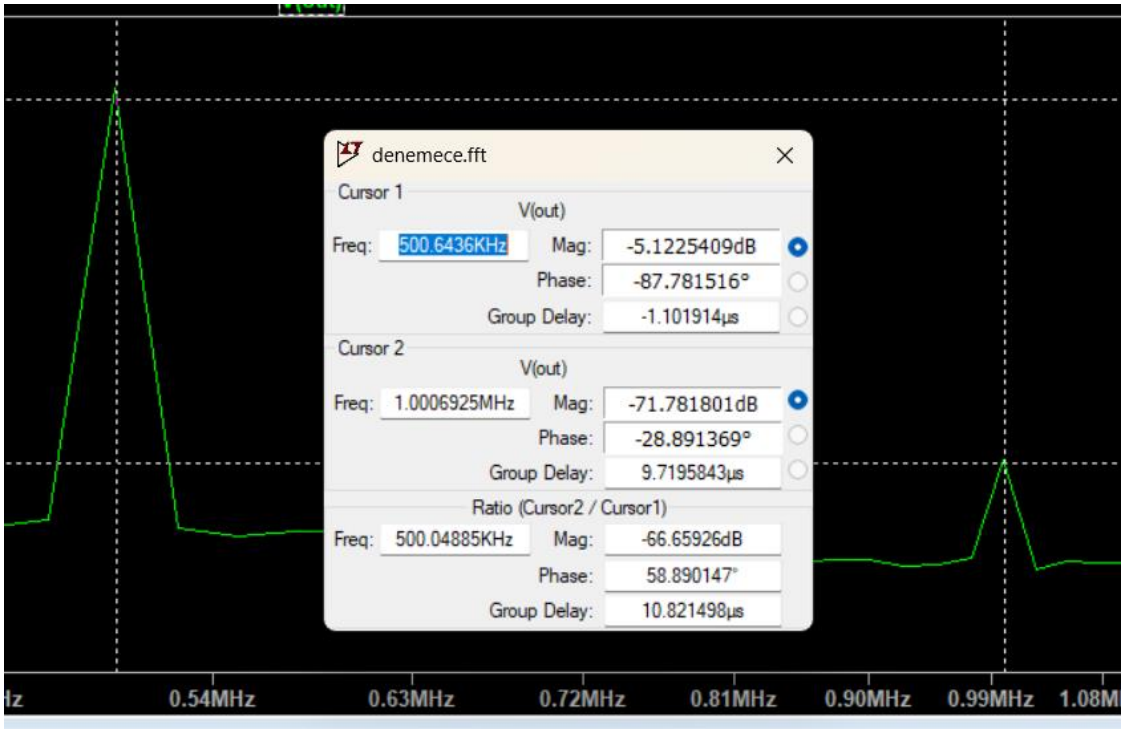

Fig. 9: dB difference between fundamental and second harmonic

Looking at the Fig. 9, dB gain at fundamental harmonic (500kHz) is -5.12 dB, at second harmonic, dB gain is -71.78 dB. The difference is -66.66dB, which is below –30dB. So, third and last specification is also satisfied.

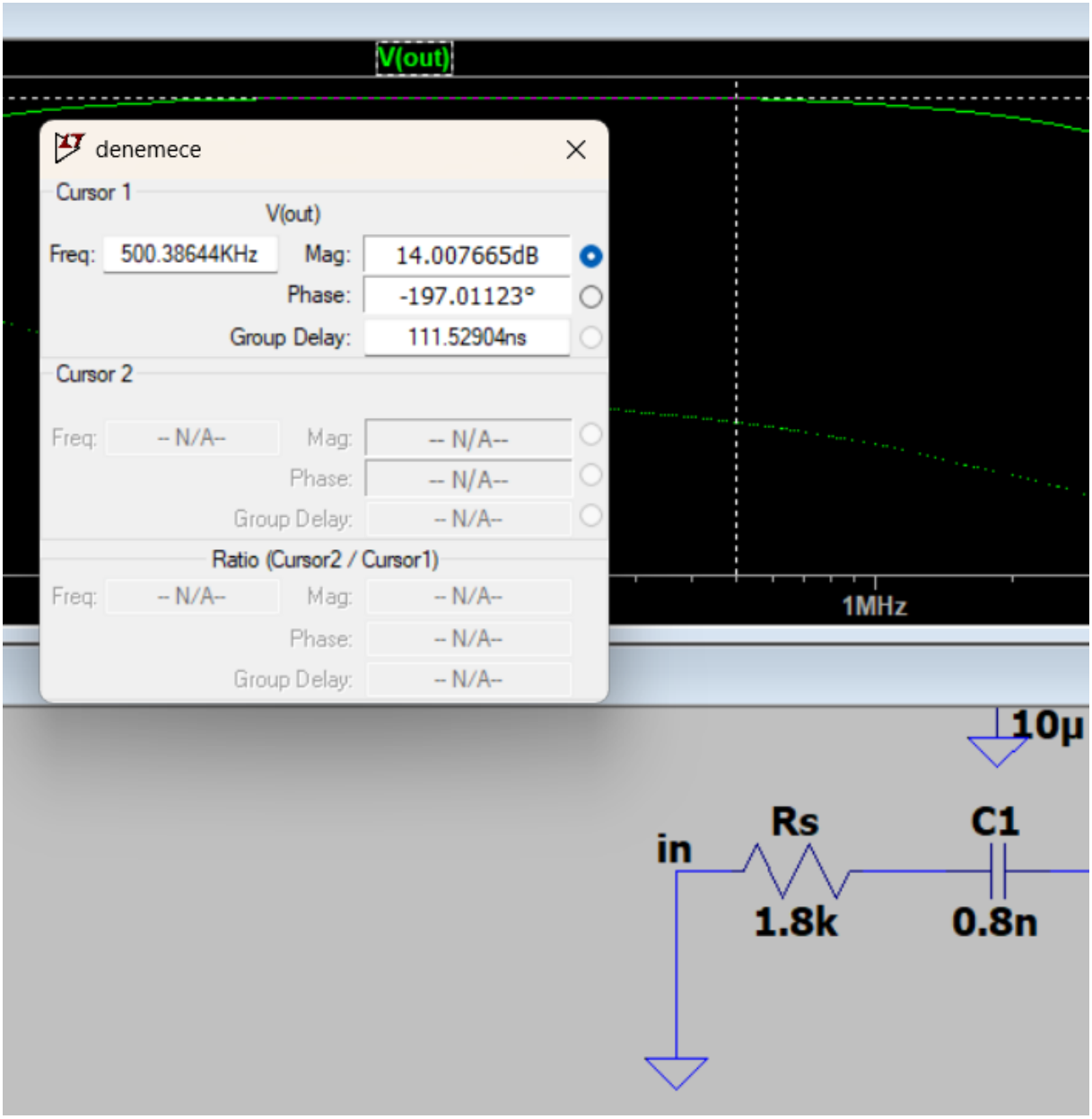

Fig. 10: Small signal input impedance value

I performed small signal AC analysis for the open-loop. Gradually increasing the value of Rs starting from 1Ω, I find the point where the dB gain is equal to 14dB. Fig. 10 shows that when Rs = 1.8kΩ, dB gain equals to 14dB. Small signal input impedance of the circuit is 1.8kΩ

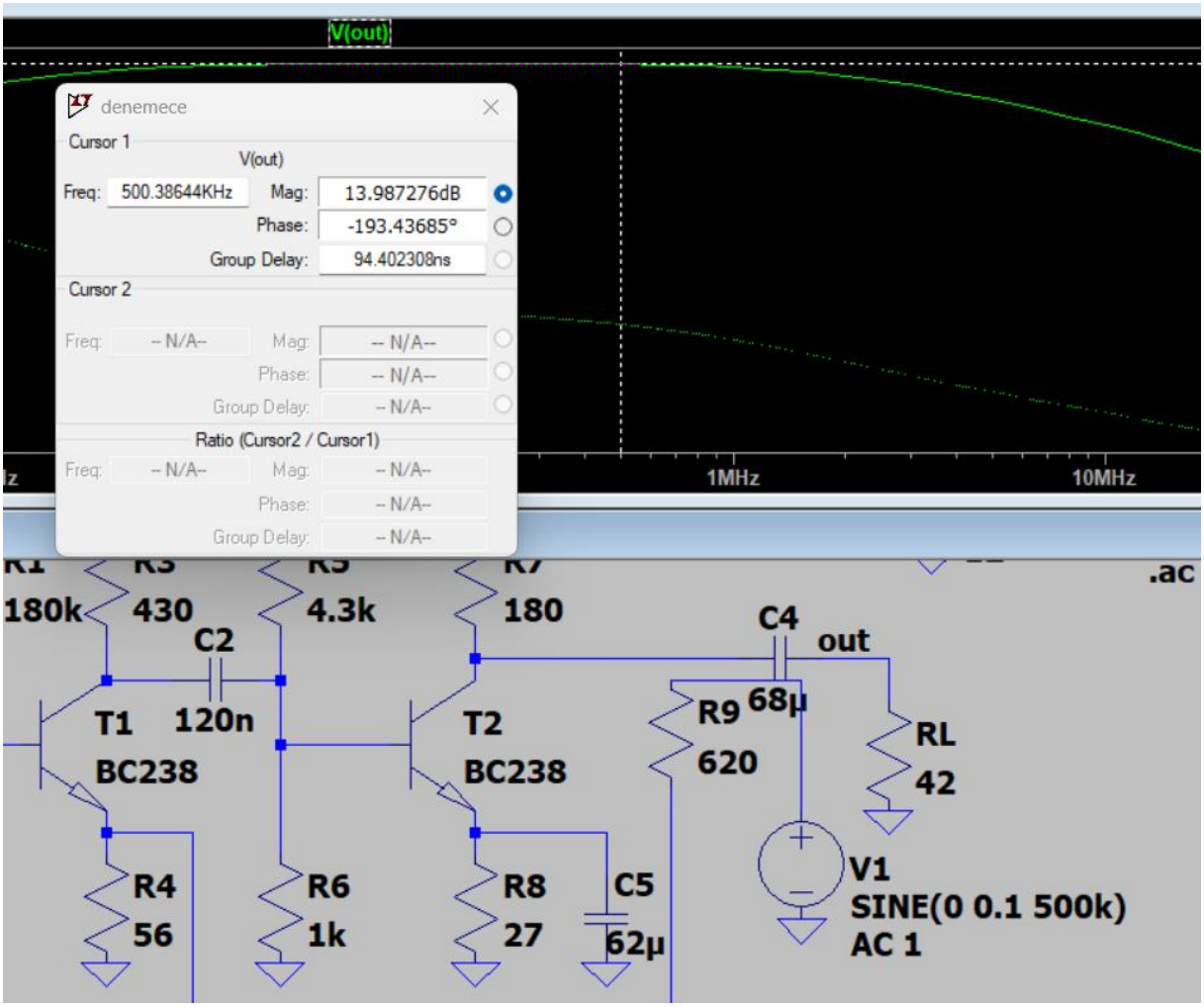

Fig. 11: Small signal input output value

Fig. 11 shows that when RL value is 42Ω, dB gain is equal to13.99dB. So, small signal output impedance of the circuit is found as 42Ω.

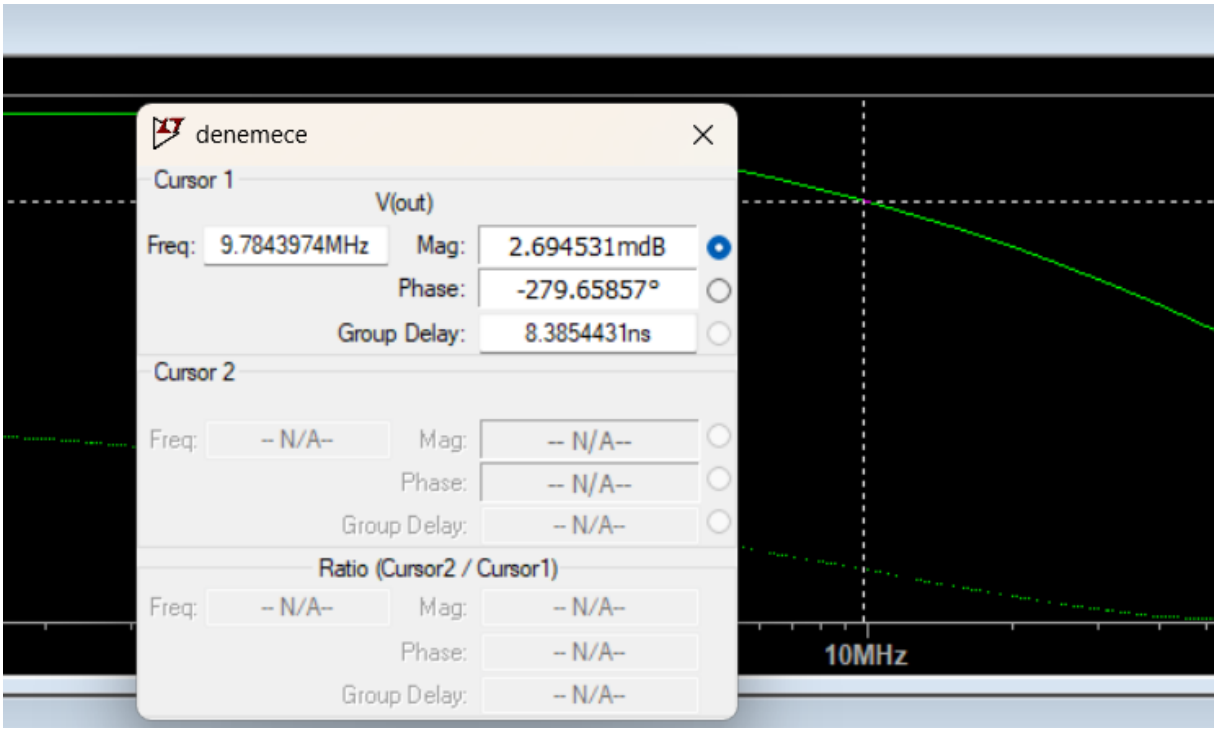

Fig. 12: Phase margin of the circuit

Looking at Fig. 12, phase margin of the circuit is calculated as -278 – (-360) = 82 degree. It is greater than 45 degree, which is what is wanted.

DipTrace schematic of the circuit is given below.

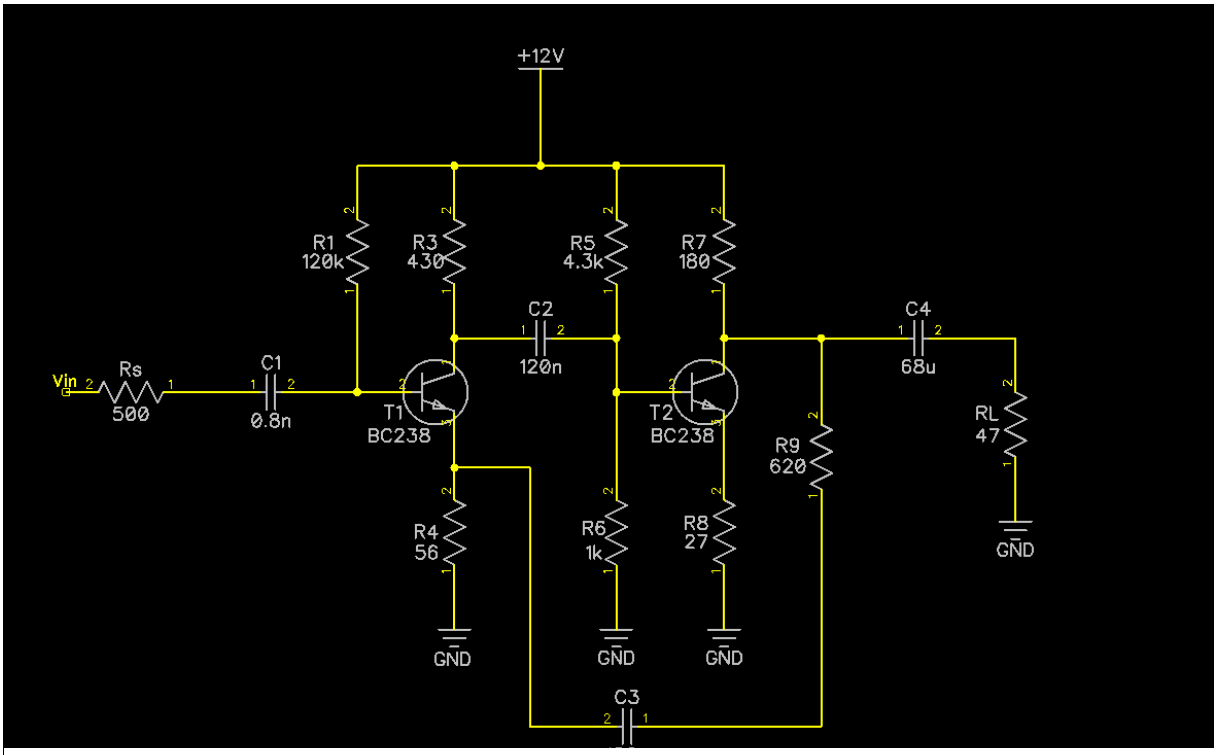

Fig. 13: DipTrace schematic

Fig. 14 shows the bill of materials.

#	RefDes	Value	Name	Quantity
1	C1, C2, C3, C4	0.8n	Capacitor, Polyester	4
2	R1, R3, R4, R5, R6, R7, R8, RL, Rs	120k	Resistor320	9
3	R9	620	Resistor420	1
4	T1, T2	BC238	BC238	2

Fig. 14: Bill of Materials