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Section: 02

Experiment Number: 04

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Lab 4 Experimental Report

Introduction

The purpose of this experiment is desinging a two-stage RC coupled amplifier with feedback. For amplification, BJT or MOS transistors will be used. Design specifications are given below.

Specifications:

1. The current consumption is less than 70mA
2. The bandwidth is at least 5KHz-5MHz while the mid-band gain is 20dB±0.5dB (measure at 5KHz, 500KHz and 5MHz). Adjust the signal generator to 50mV peak (meaning it generates 200mV peak-to-peak) and insert a 470Ω resistor in series with the signal generator to simulate R_S=500Ω. The output voltage across R_L=47Ω should be 2V peak-to-peak.

3. The harmonic content of the output voltage is beΣer than −30dBc at 500KHz.

Methodology

I built the circuit on the breadboard. To get the desired results, I adjusted the value of 120nF capacitors to 560nF capacitors. Also I decreased the gain ratio in the hardware to get 2V pk-pk at the output.

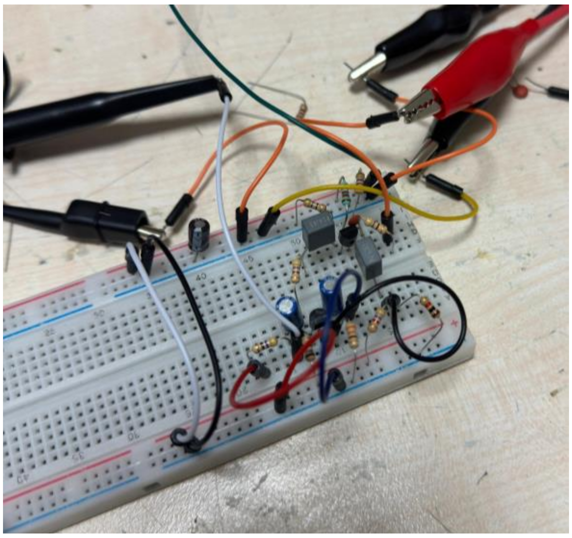


Fig. 1: Designed circuit built on breadboard

Analysis

First Specification:

Throughout the experiment, I used 0.2V pk-pk input sine wave signal with various frequency values. For f=500kHz, current of supply voltage is 62mA (Fig. 2), which is less than 70mA.

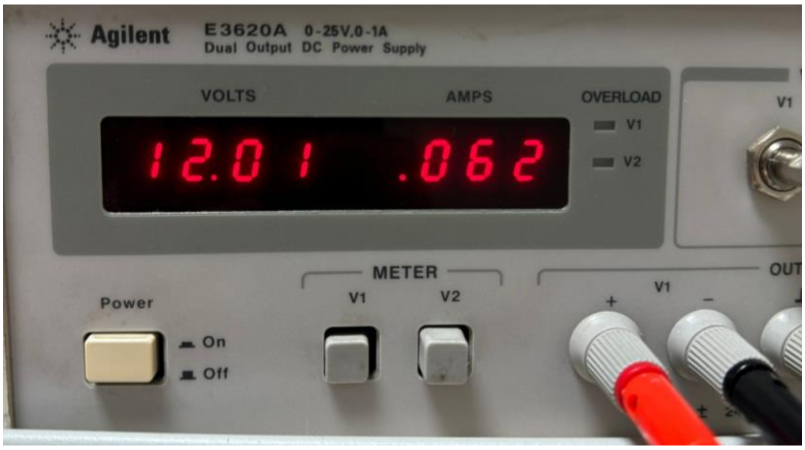


Fig. 2: Current of supply voltage

Therefore, first specification was satisfied.

Second Specification:

For this part, the bandwith of the amplifier is measured. In LTspice, a flat gain of 20.5 dB is achieved from 7kHz to 11MHz. In hardware part, dB gain is measured at 5kHz, 500kHz, and 5MHz. The next three figures show the output signals respectively.

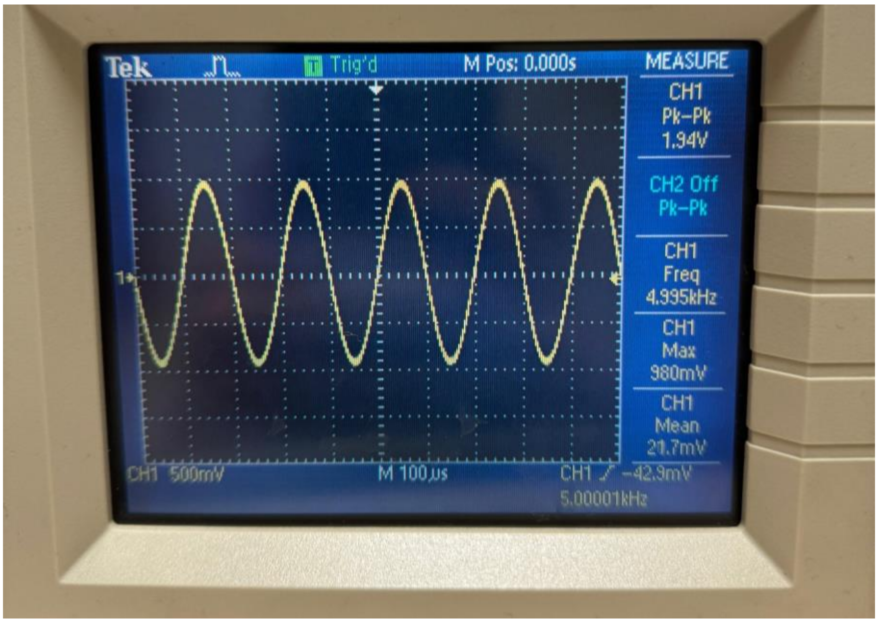


Fig. 3: Output voltage at f = 5kHz

At 5kHz, output voltage is 1.94V pk-pk.

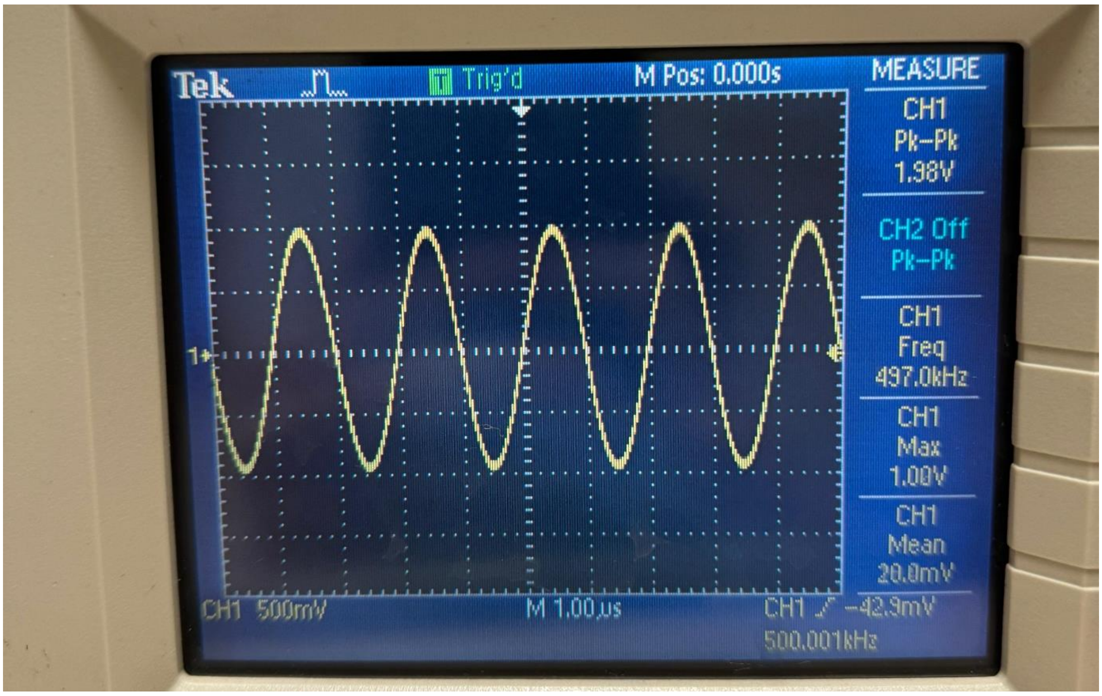


Fig. 4: Output voltage at f = 500kHz

At 500kHz, output voltage is 1.98V pk-pk.

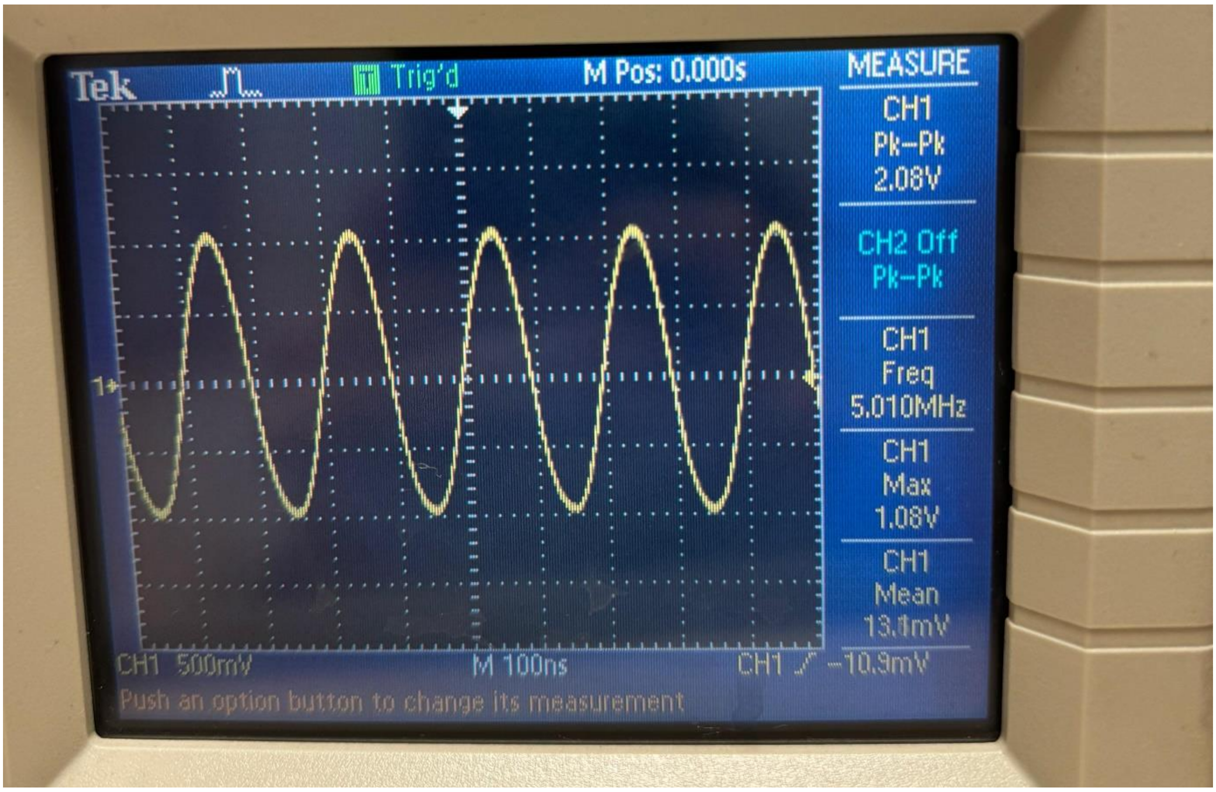


Fig. 5: Output voltage at f = 5MHz

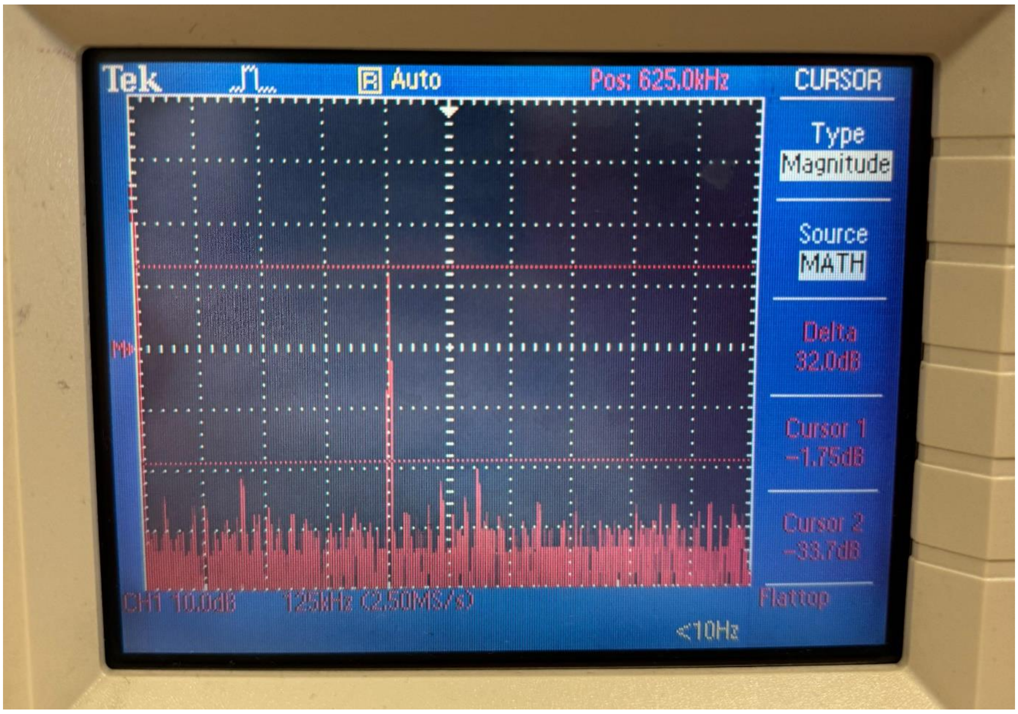
At 5MHz, output voltage is 2.08V pk-pk.

Overall, a flat gain is achieved with slight increase and decreases in the output voltage from 5kHz to 5MHz. The differences may be caused by capacitors and signal generator’s insensitiveness.

Second specification was satisfied.

Third Specification:

Fig. 6 shows the FFT graph of the circuit. From there, it is seen that second harmonic (1MHz) has a magnitude of -33.7dB, and the difference between second harmonic and fundamental (500kHz) signal is 32.0dB.



Third specification was satisfied.

To find small-signal input and output impedances of the circuit, I tried some resistor values at R_s and R_L. I tried to find which resistor value gives me -3dB point since it is wanted to find the resistor value that makes the voltage half of the input voltage. By this logic, actually it is not necessary to try various resistor values because the equation is already known and given below.

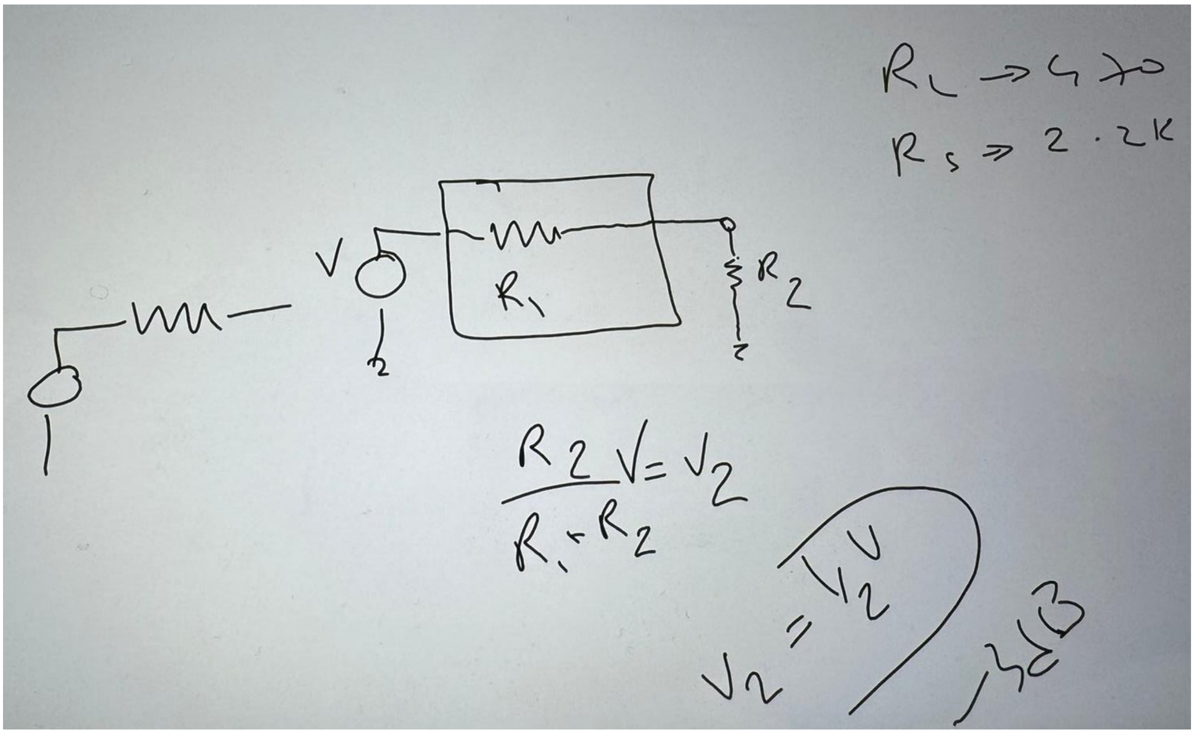


Fig. 6: Equation for R_S and R_L

However, -3dB point is achieved when R_S = 2.2kΩ and R_L = 470Ω.

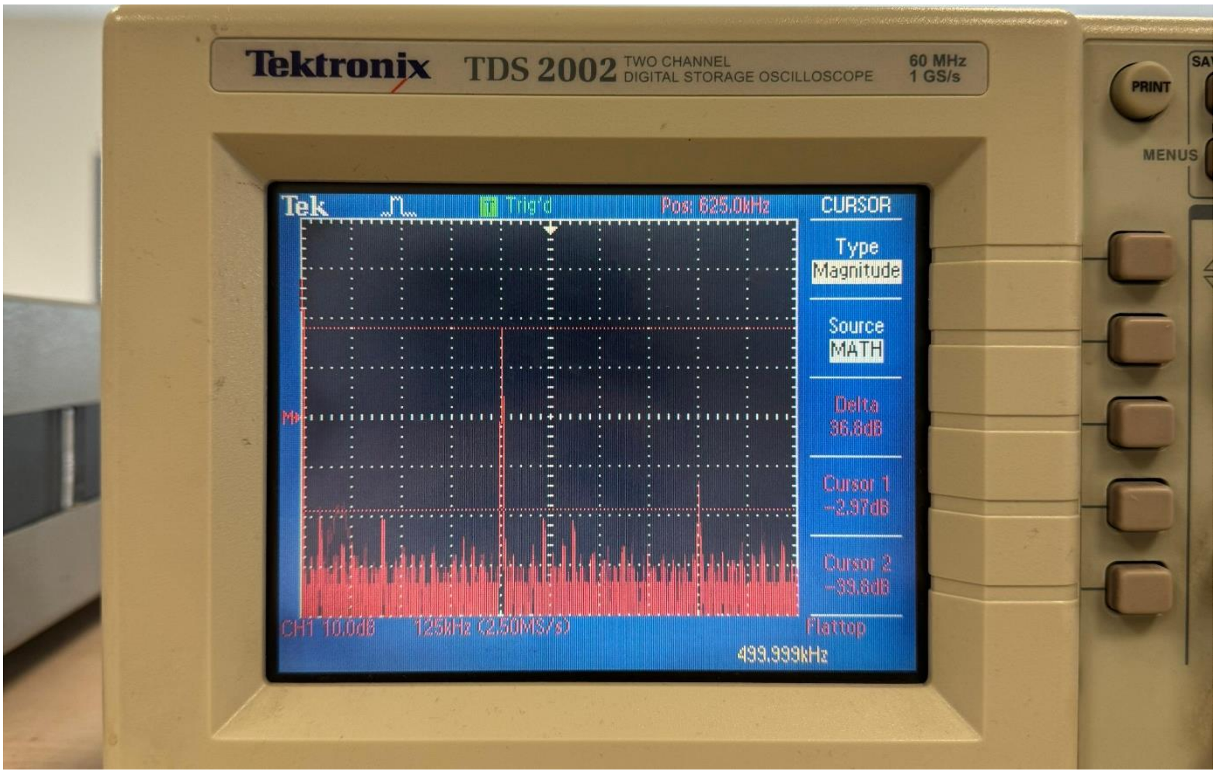


Fig. 7: FFT for R_S = 2.2kΩ

As seen from Fig. 7, gain is -2.99dB.

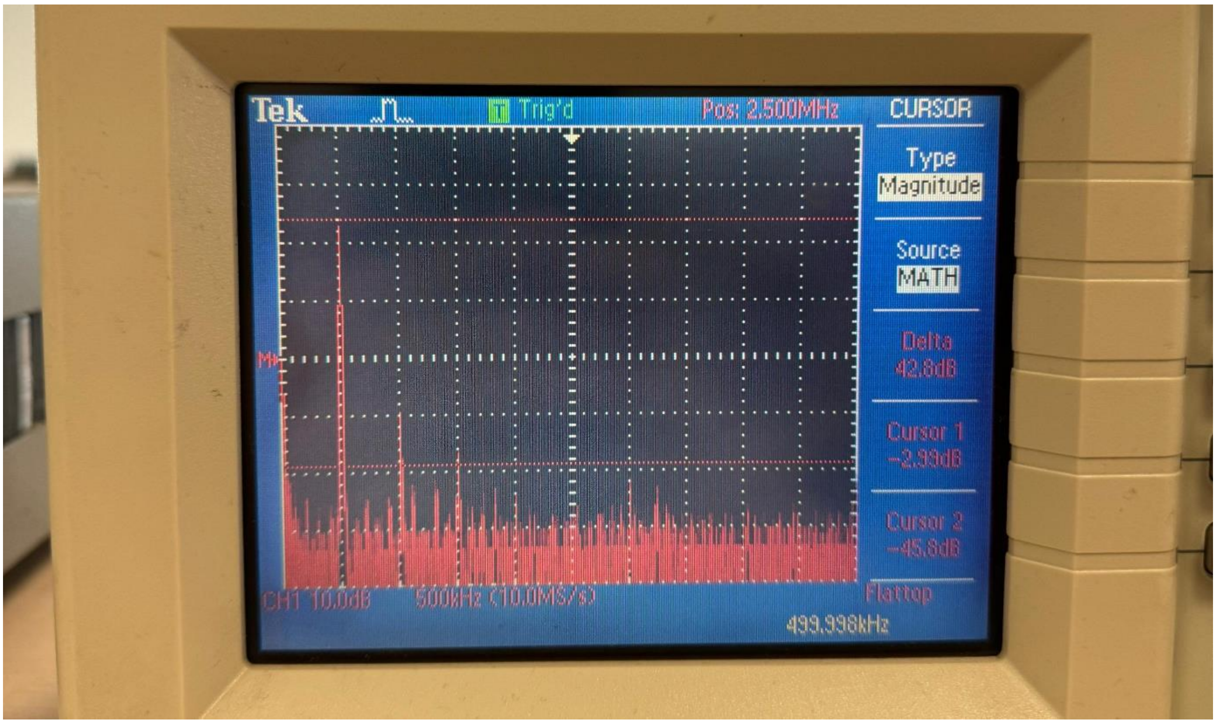


Fig. 8: -3dB point for R_L = 470

As seen from Fig. 8, gain is -2.97dB.

In simulation, R_S value was found as 1.8kΩ and R_L value waas found as 42Ω. In hardware part, R_S value is nearly same, 2.2kΩ, however, R_L values are different from each other.