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EEE419 Lab 1 Preliminary

Introduction:

In this experiment, a half-bridge isolatedd DC-DC converter is designed. The input voltage V_d will be chosen less than 30V and according to that, an output voltage V_O, less than 50V, is going to be delivering 2W to the chosen load resistor R_L.

Methodology:

First, the input voltages for the half-bridge driver (IR2109) are generated using a NE555 and a pnp transistor which inverts the output. The NE555 generates pulse with duty cycle greater than 0.5. Using a pnp transistor, the signal can be inverting. Therefore a pulse with a duty cycle less than 0.5 can be obtained. The calculated duty cycle is 0.2, so, for the $\overline{SD}$ signal, it is wanted to have a pulse with the twice value of the desired result which is D=0.4. Fig. 1 shows the graph of the $\overline{SD}$ signal. The T_S is measured as 11.8µs and t_{ON} times measured as 4.8µs. The corresponding duty cycle D is 0.406. To obtain this value, the following equation is used for choosing the resistor values.

$$D = \frac{R_B}{R_A + 2R_B}$$

$$R_B = 6.8K\Omega$$
$$R_A = 3.3K\Omega$$

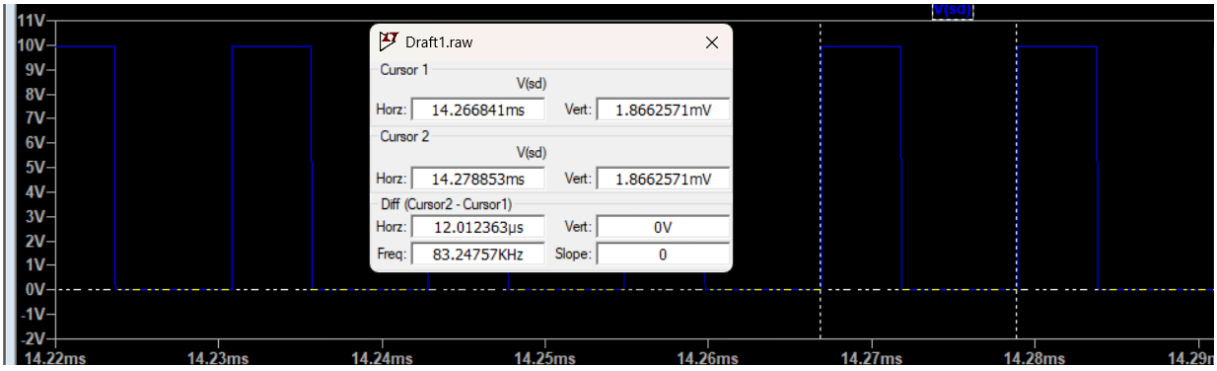

Fig. 1: T_S time for NE555 output

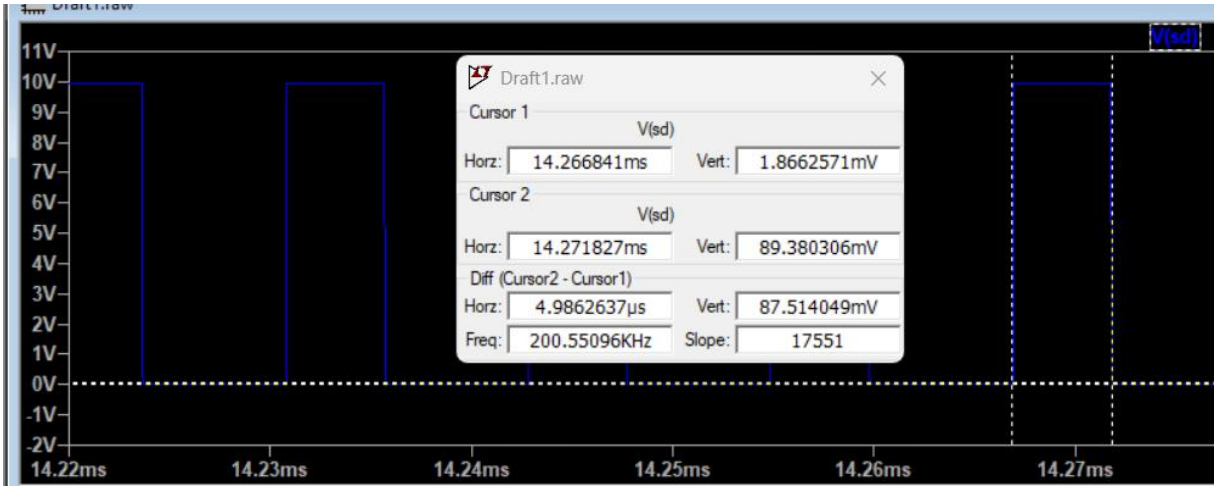

Fig. 2: t_{ON} time for NE555 output

The duty cycle of the generated pulse is calculated as $\frac{4.98}{12.01}$=0.415, which is valid because this is the twice of the value I needed which is D=0.2.

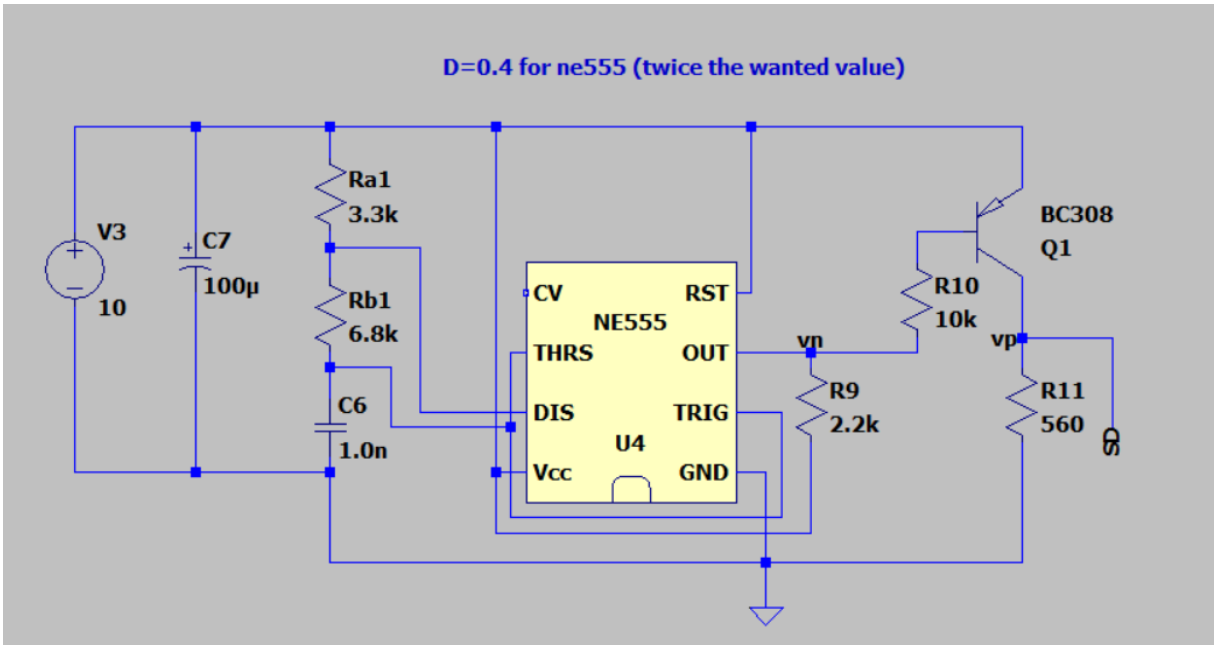

Fig. 3: NE555 and pnp transistor circuit

Fig. 3 shows the pulse generator of the circuit with D less than 0.5 because a pnp transistor is used to invert the output.

To obtain IN signal, a negative (falling) edge triggered counter is used. It basically counts the falling edges of a pulse and each time it counts, it flips (complements) the digital signal. Fig. 4 shows the graph of IN signal with $\overline{SD}$ signal together.

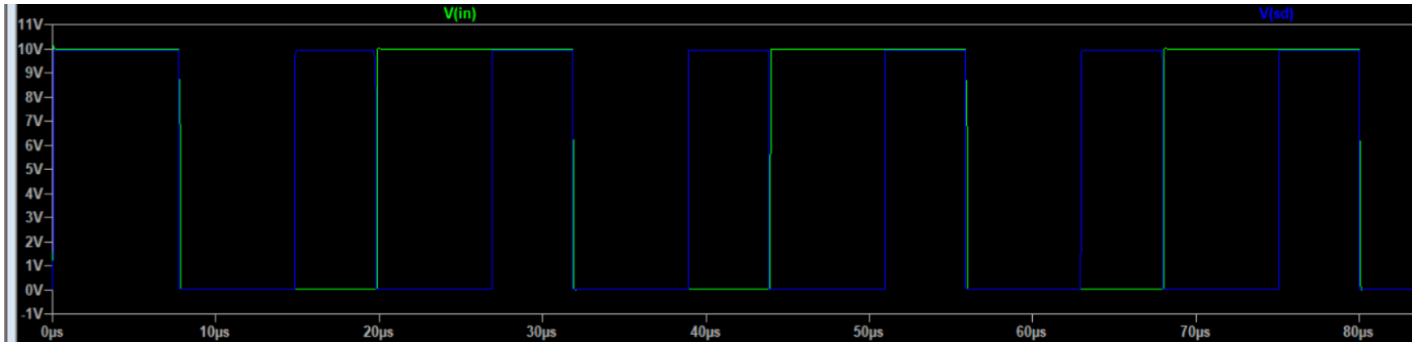

Fig. 4: $\overline{SD}$ and IN signal

When IN is low-level and $\overline{SD}$ is high-level, only T_2 is ON. When IN and $\overline{SD}$ both are high-level, only T_1 is ON.

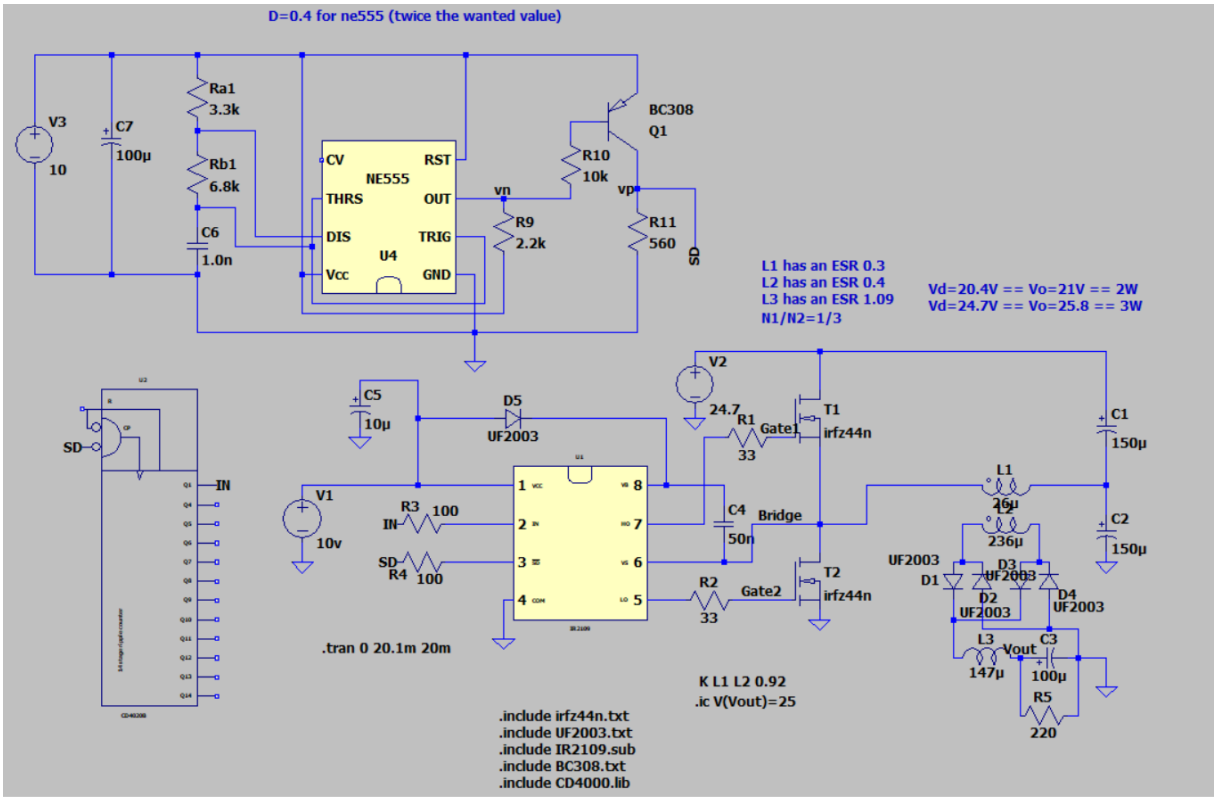

Fig. 5 Designed Circuit Schematic:

Analysis:

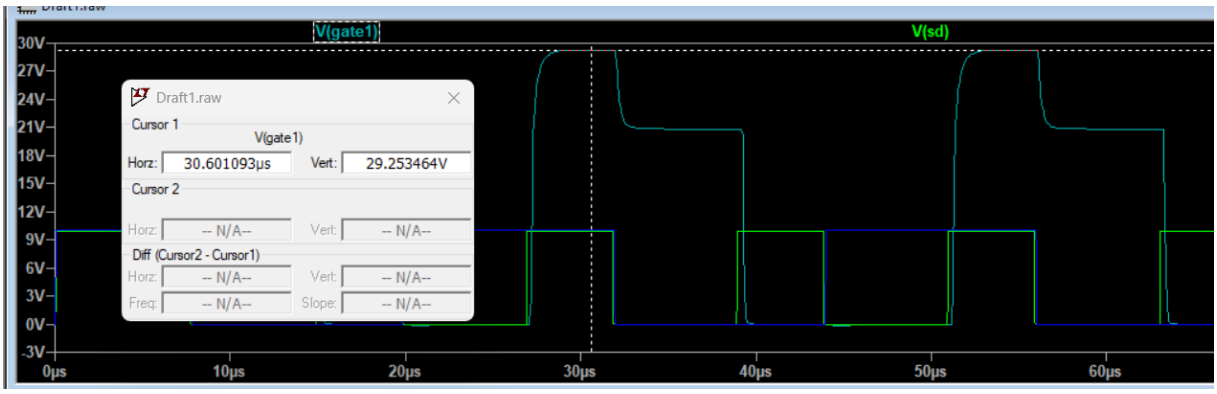

Fig. 6: Gate voltage of T_1 (Green line)

In Fig. 6, where both IN and $\overline{SD}$ signals are high-level, T_1 is ON,The voltage is measured as 29.25V. Theoretically, the voltage value should be V_d+10V=30.4V. I think the difference between the measured and theoretical values may be caused by the losses included in the circuit. When both switches are OFF, the voltage reduce to 20.8V. Finally, when only T_2 is ON and T_1 is OFF, the voltage reduces to 0V.

In Fig. 7, when only T_2 is ON, the gate voltage is equal to 10V. When only T_1 is ON, gate voltage is equals to 0V.

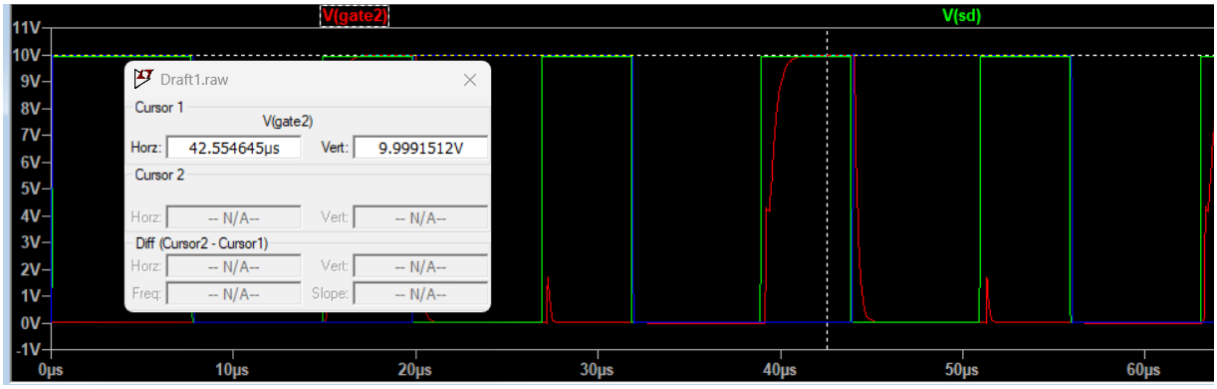

Fig. 7: Gate voltage of T_2 (Green line)

The bridge voltage is measured as 20.4V which is equal to V_d as expected.

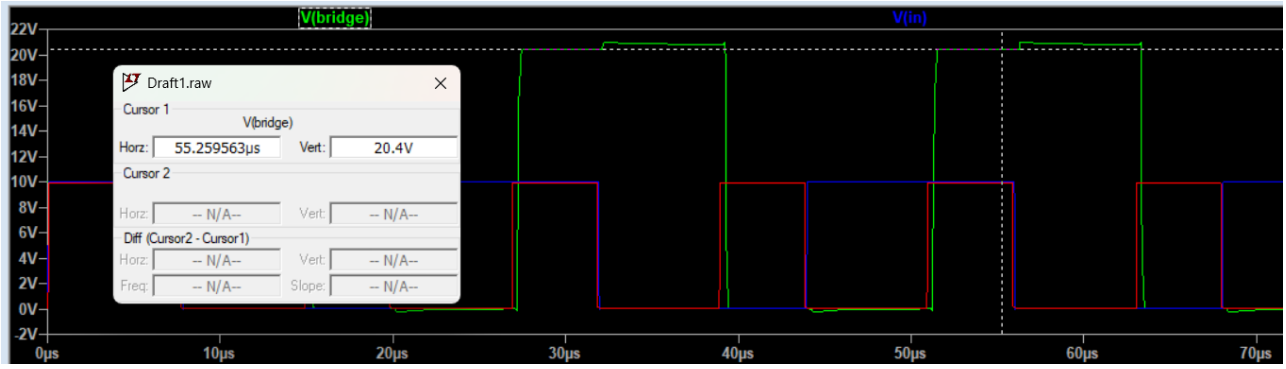

Fig. 8: Bridge voltage

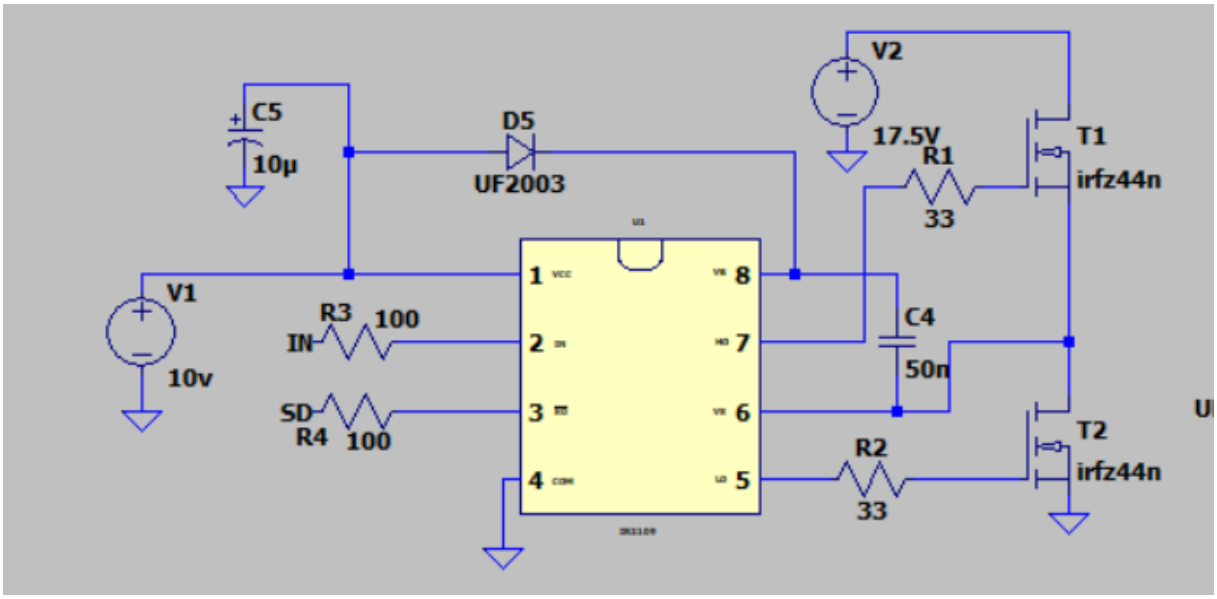

Fig. 9: IR2109 half-bridge driver circuit

The series resistors of the transformer are added (0.3Ω for primary and 0.4Ω for secondary windings) and currents of the transformer are observed.

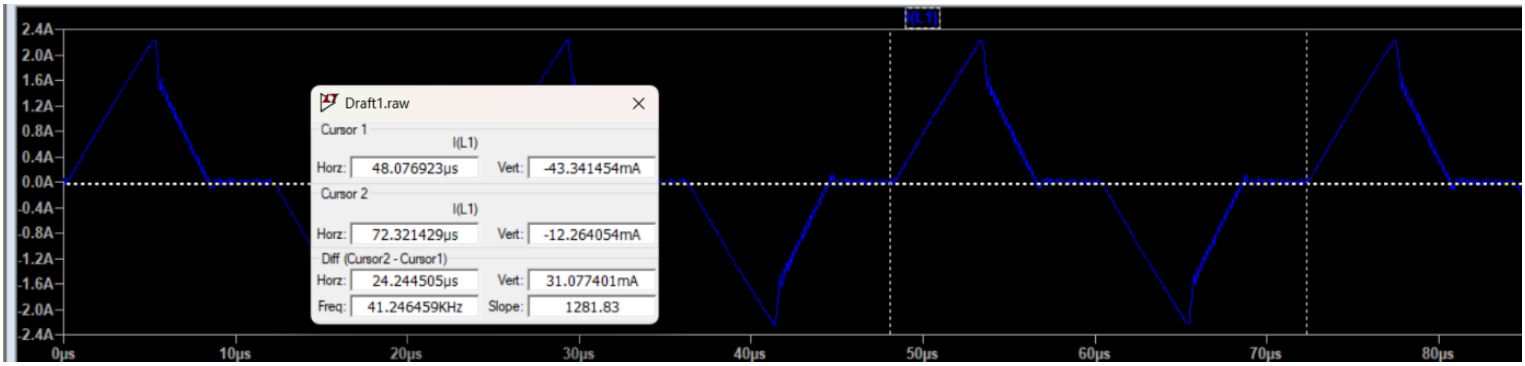

Fig. 11: Primary winding inductor current graph

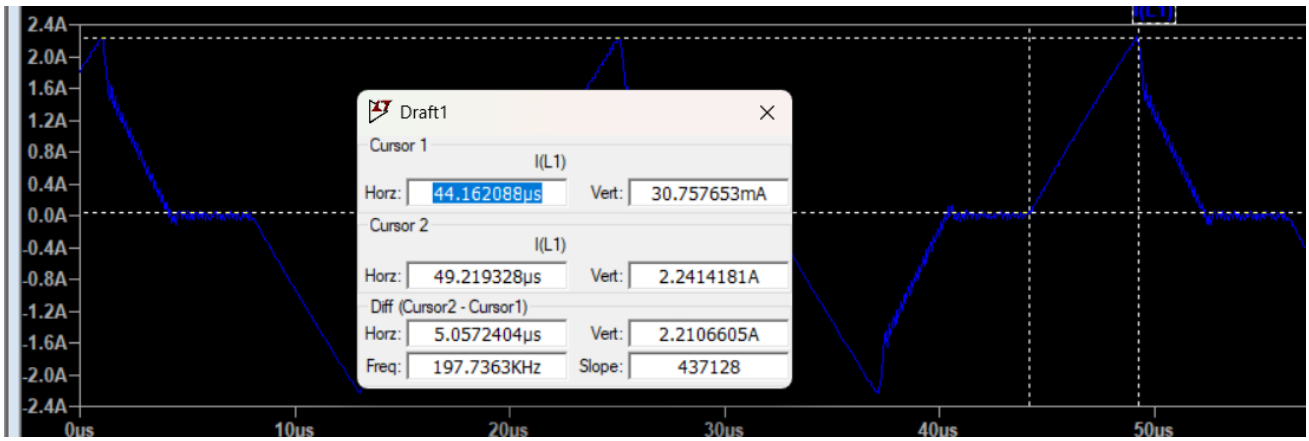

Fig. 10: DT_S = 5.05µs

The 2A peak current is obtained when (D1-D4, L1, C3, and load resistor) are not connected to the secondary winding of the transformer. The figure above shows the inductor current for primary when the circuit is completed. Therefore the peak current is about 2.2A. As seen from the figure, the period of the circuit is measured as 24.2µs. The DT_s value is 5.05µs. Therefore, the duty cycle D is calculated as 0.2 as expected.

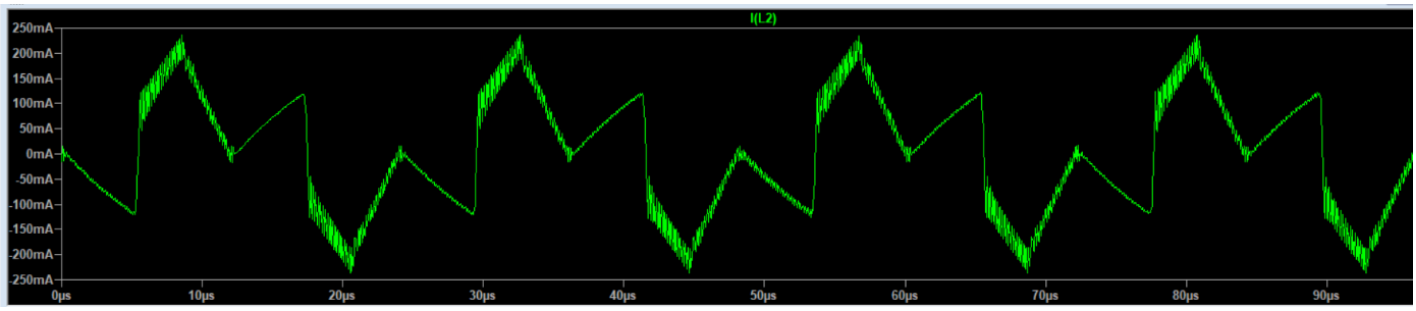

Fig. 12: Inductor current of the secondary winding in PSS

I choose the load resistor as 220Ω. To obtain 2W at the output, I calculated the output voltage V_O to be 21V. Also, I adjusted the repetition period to limit the current of the primary side of the inductor current to be less than 2A. So the peak value of the inductor current is around 2A. Using the following equation with D=0.2, R_L=220Ω, i_{mpeak}=1.9A, and N_2/N_1=3, the input voltage V_d will be determined.

$$V_O = \frac{2V_d \frac{N_2}{N_1} D}{1 + \frac{N_2/N_2}{R_L i_{mpeak}} V_d \frac{N_2}{N_1} D}$$

From this equation, V_d value is found as 18.9V. However, when I simulated with this input voltage value, I cannot get the desired power at the output. Therefore, I increased the input voltage V_d to 20.4V. The graph below shows the output voltage when V_d=20.4V. As seen, in PSS, the output voltage V_O value is 21.05V.

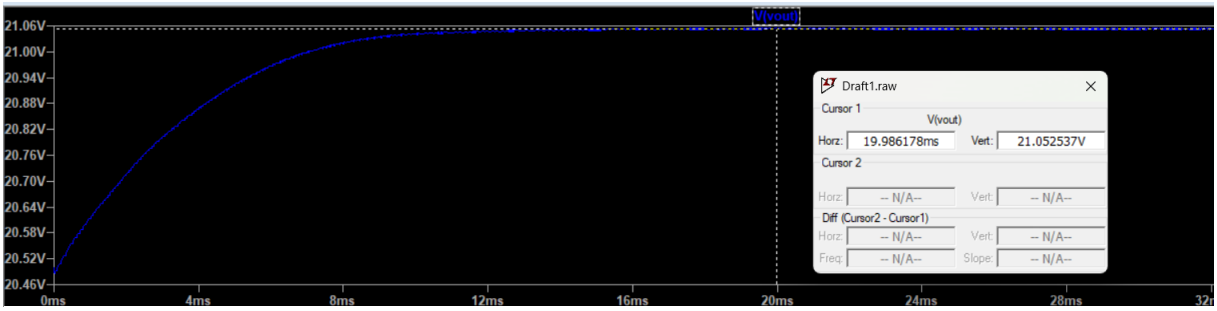

Fig. 13: Output voltage graph

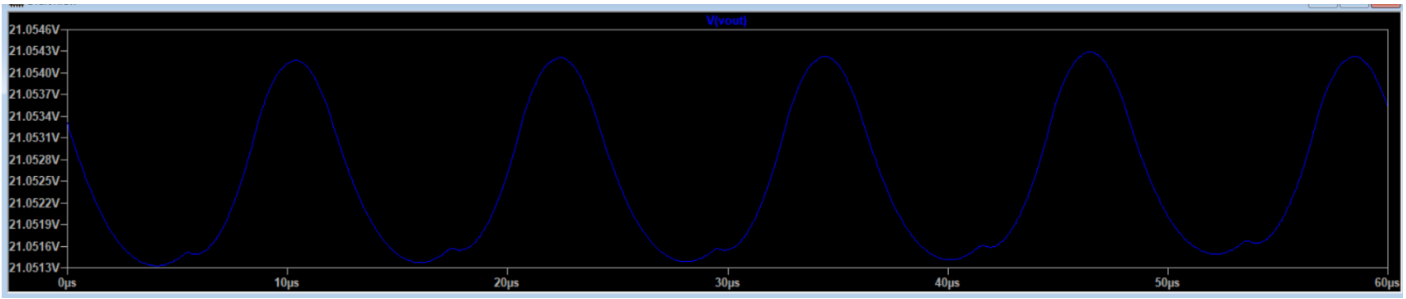

Fig. 14: Zoomed in version of V_O

As seen from Fig. 15, the output power P_O is 2.01W in PSS. The desired result is obtain.

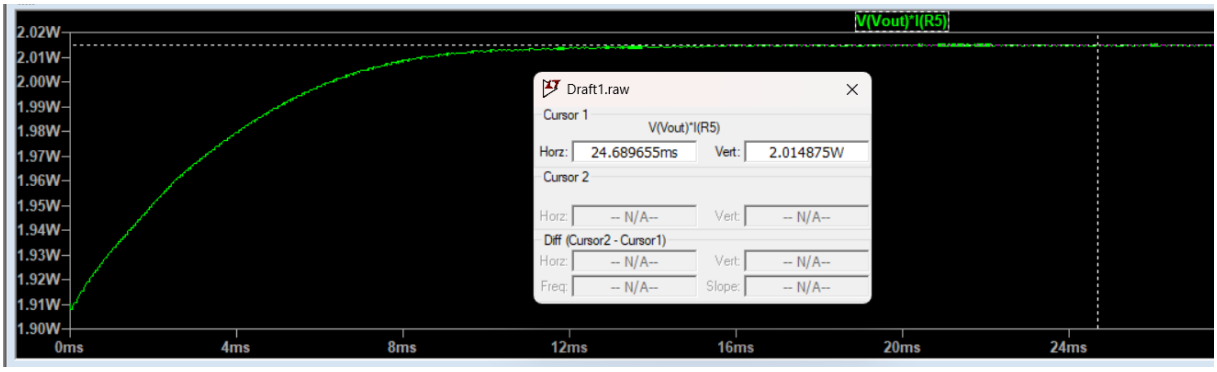

Fig. 15: Output power

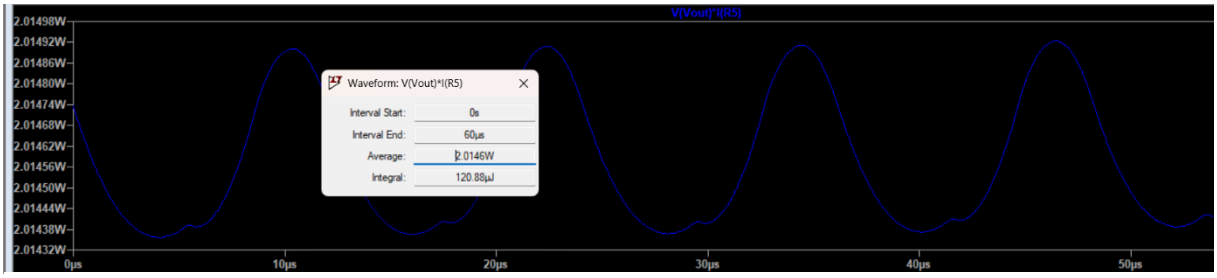

Fig. 16: Output power

The output power of the circuit when integer number of cycles are generated is measured as 2.014W.

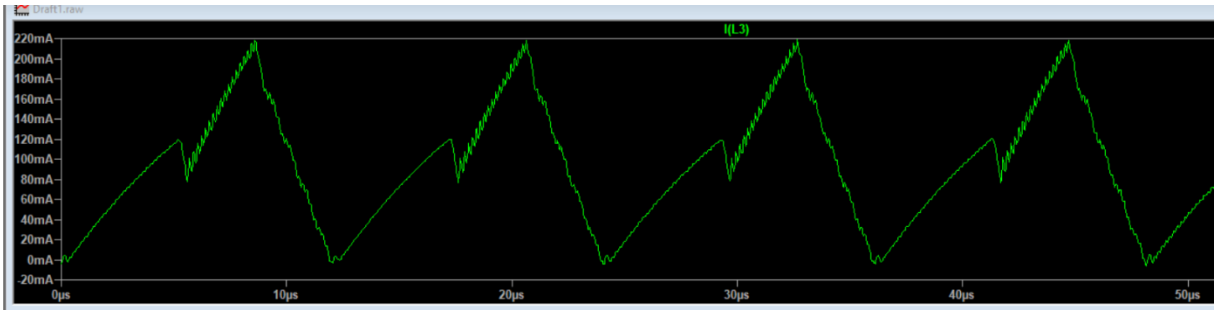

Fig. 17: Output inductor current graph in PSS

To get 3W at the output, the output voltage has to be 25.7V. The adjustments are made to the V_d to get the desired results.

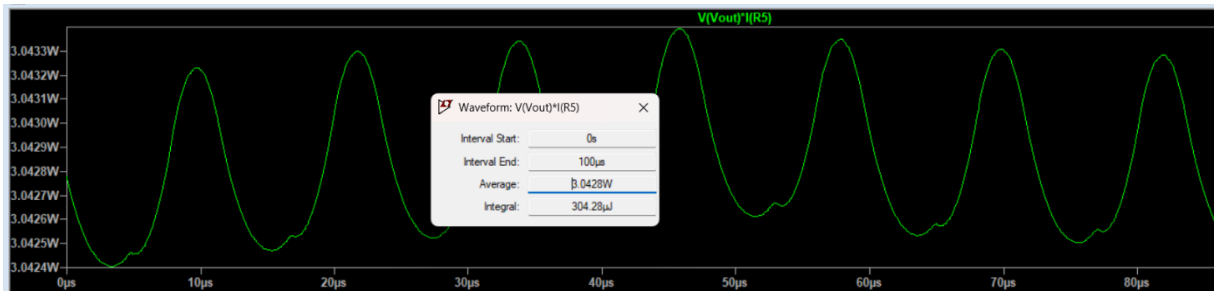

Fig. 18: 3W output power

The V_d value is determined as 24.7V by trial-error.

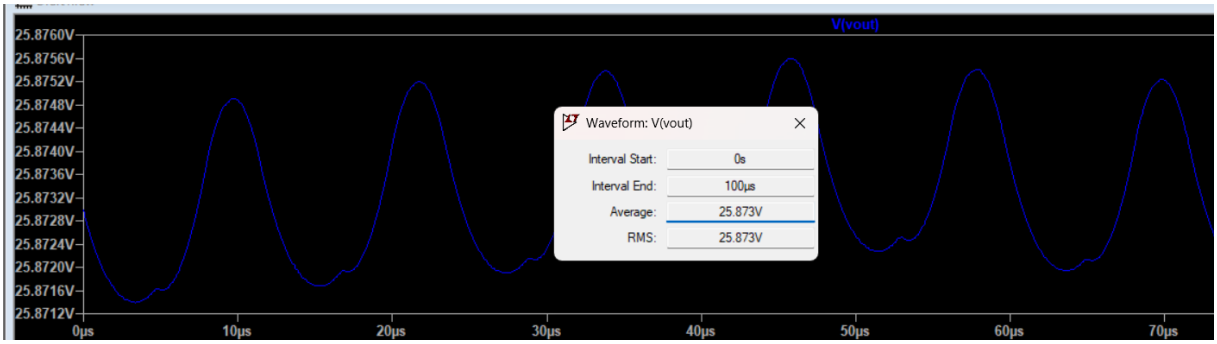

Fig. 19: Output voltage when PO=3W

The wanted value is calculated as 25.7V and in the simulation, the value is measured as 25.8V.

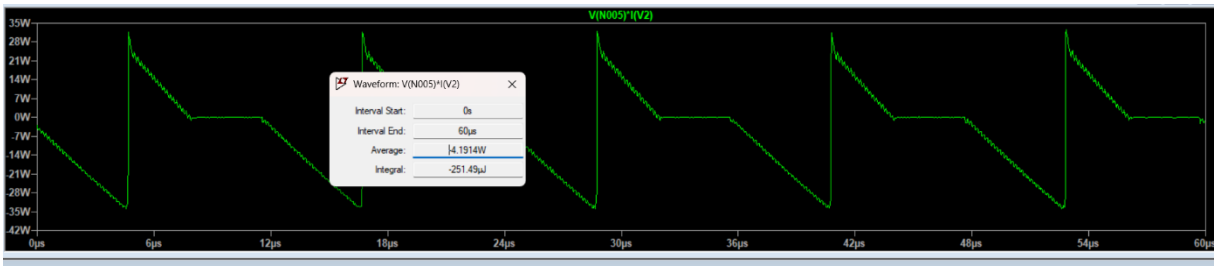

Fig. 20: Input power

The input power P_{IN} is measured as 4.19W when there are integer number of cycles present. The output power P_O is measured as 3.04W. The efficiency of the circuit is calculated as 73%.

$$\eta = \frac{P_O}{P_{IN}} * 100 = 73\%$$