Full Name: Orkun İbrahim Kök

Department: EEE

Course Code: EEE202

Section: 02

Experiment Number: 04

Date: 26.11.2023

Lab 4 Report

Software Implementation

Introduction:

The purpose of this experiment is to design a circuit that generates a waveform similar to Figure 1. The peak value of the waveform should be 7V and input voltage is 5V peak-to-peak square wave. Delays can also be seen in Figure 1. Input frequency is chosen a 25Hz which is less than 50Hz.

$$\Delta t_0 = 3ms$$

$$\Delta t_1 = 3ms$$

$$\Delta t_2 = 2ms$$

$$\Delta t_3 = 2ms$$

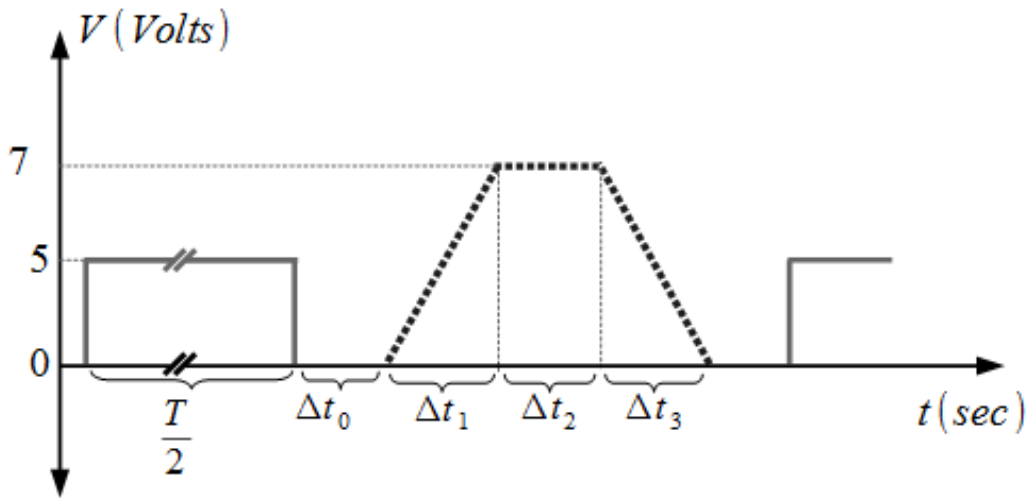

Figure 1: Desired Waveform

In order to obtain a waveform similar to one in the Figure 1, OPAMPs are going to be used. The VCC of the LM-324 OPAMPs are going to be fed with 8.5V DC input in order to get 7V voltage as maximum.

Analysis:

3 different type of OPAMPs used in the experiment are listed above:

- Comparator OPAMP
- Integrator OPAMP
- Subtractor OPAMP

Comparator OPAMP

The main purpose of a comparator OPAMP is comparing the voltages at inverting and non-inverting poles of the OPAMP, and chooses the larger one as the output voltage. Therefore, I pick a RC value in order to find when will the capacitor in the inverting OPAMP will reach 1V. When the capacitor reaches 1V, approximately 3ms will elapse. The same calculations will be done in order to obtain 10ms delay.

First order ODE for capacitors of OPAMP:

$$\frac{dV_C}{dt} \times C = \frac{5 - V_C}{R}$$

$$\frac{dV_C}{dt} \times C + \frac{V_C}{R} = \frac{5}{R}$$

Characteristic Equation:

$$\lambda + \frac{1}{RC} = 0$$

Equation of capacitor for t≥0:

$$V_c(t) = A * e^{\frac{-t}{RC}} + 5$$

When t=0, $V_C(0)$ = 0V, then A value could be found as:

$$V_c(0) = 0 = A * e^{\frac{-t}{RC}} + 5$$

$$0 = A + 5$$

$$A = -5$$

At t=3ms, V_C = 1V as the non-inverting output of the OPAMP.

For 3ms delay:

$$-5 * e^{\frac{-t}{RC}} + 5 = 1$$

$$e^{\frac{-3ms}{R_1 C_1}} = \frac{4}{5}$$

$$R_1 * C_1 = 0.0134$$

$$R_1 = 10K\Omega;\ C_1 = 134nF$$

For 11ms delay:

$$-5 * e^{\frac{-t}{RC}} + 5 = 1$$

$$e^{\frac{-10ms}{R_2 C_2}} = \frac{4}{5}$$

$$R_2 * C_2 = 0.0448$$

$$R_2 = 10K\Omega;\ C_2 = 450nF$$

However, there is one thing that I want to add. Using the theoretical calculated values, the desired delays cannot be achieved immaculately because every OPAMP used in the circuit adds some delay regardless. Therefore, I made some alterations after finding the R and C values in order to obtain the desired delays. For example, I used 4.7KΩ resistor and 340nF, then, $RC = 0.016$, whereas, the calculation showed us $RC = 0.0134$. The difference between these two values are shown in the below figures.

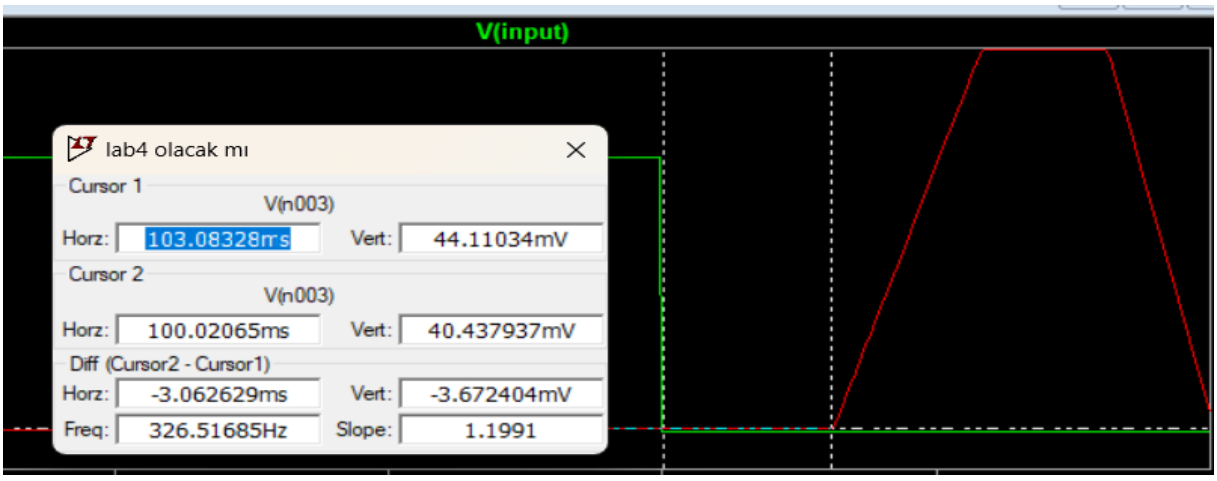

Figure 2: R = 4.7KΩ; C = 340nF; $RC = 0.016$; delay = 3.06ms

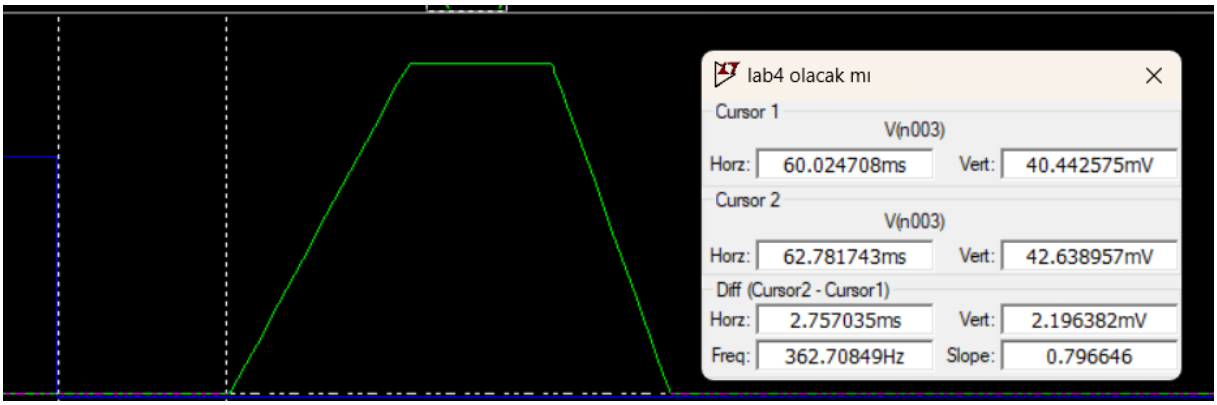

Figure 3: R = 10KΩ; C = 134nF; $RC = 0.0134$;delay = 2.75ms

As in 3ms delay, I also made some alterations in order to obtain immaculate 10ms delay. The calculated theoretical value for $RC = 0.0448$ shows us delay to be 9.56ms. Playing a little bit with R and C values, $RC = 0.0489$ value is achieved and delay turned out to be 10.09ms. The differences can be seen in the figures below.

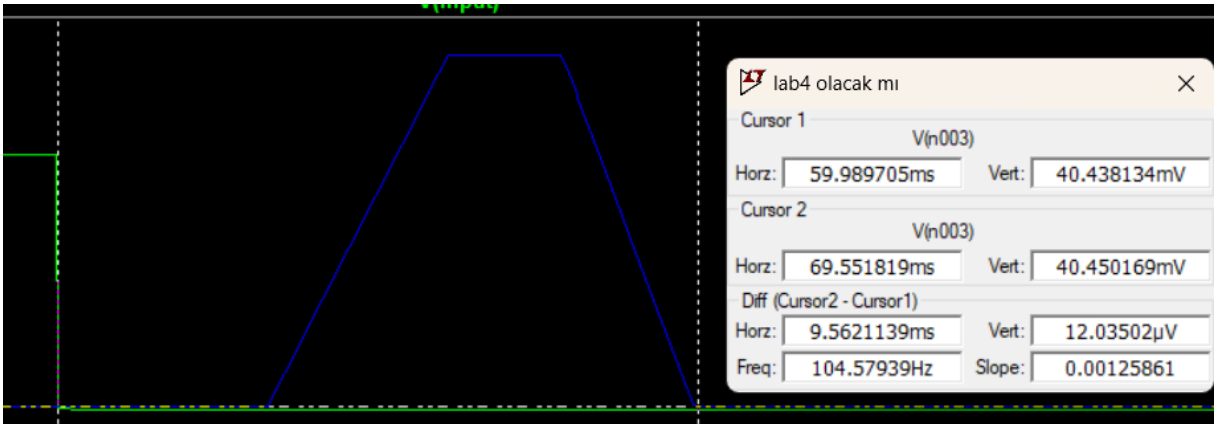

Figure 4: R = 10KΩ; C = 450nF; $RC = 0.0448$; delay = 9.56ms

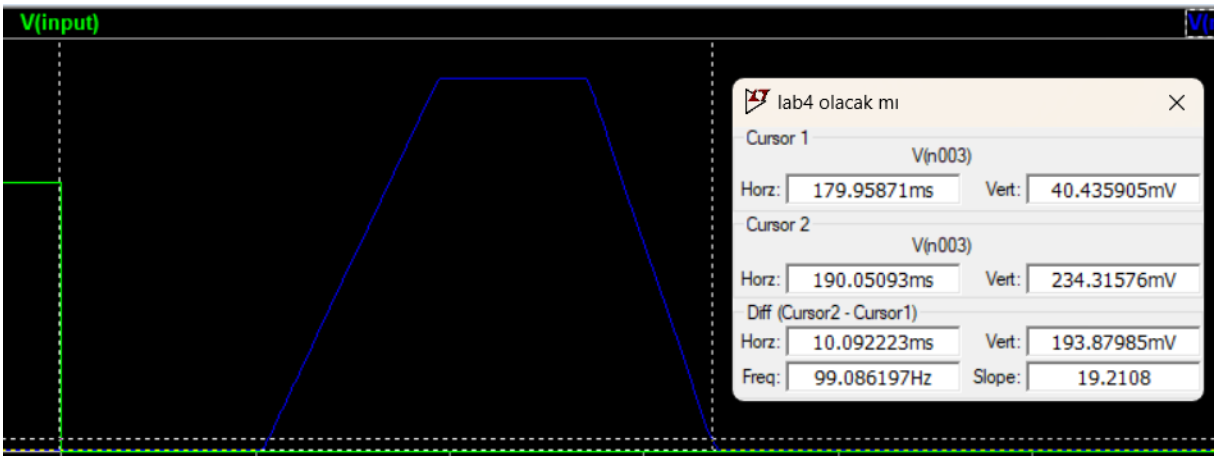

Figure 5: R = 8.8KΩ; C = 556nF; RC = 0.0489; delay = 10.09ms

Resistor	Capacitor	RC	Time Delay	Error
10K	134nF	0.0134	2.75ms	9.1%
4.7K	340nF	0.016	3.06ms	1.96%

Table 1: Error calculation for 3ms delay of comparator 1

Resistor	Capacitor	RC	Time Delay	Error
10K	450nF	0.0448	9.56ms	4.6%
8.8K	556nF	0.0489	10.09ms	0.89%

Table 2: Error calculation for 10ms delay of comparator 2

Looking at (Table 1) and (Table 2), calculated results are lying inside the error bound which is 10% for software implementation.

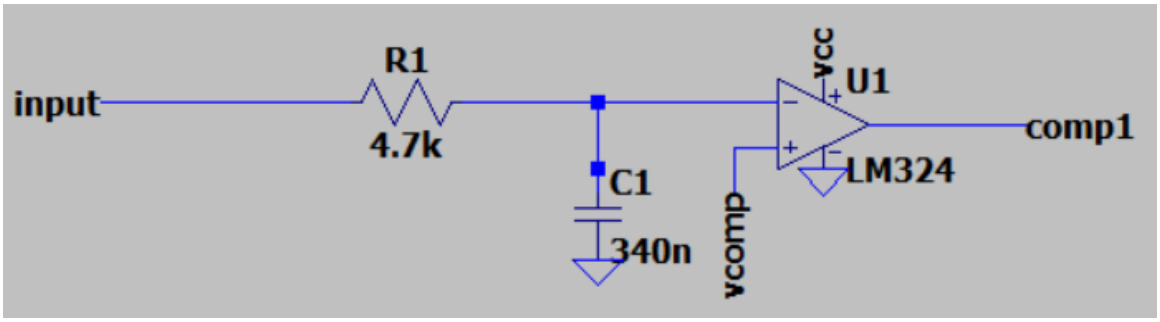

Figure 6: Comparator 1

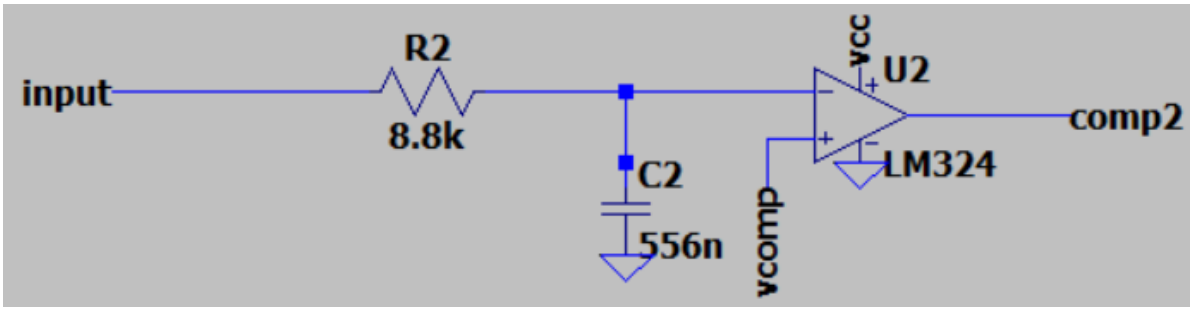

Figure 7: Comparator 2

Integrator OPAMP

From KCL:

$$\frac{V_{input} - V_+}{R} = C\frac{dV_C}{dt}$$

$$V_{input} = 7V$$

$$V_+ = 1V$$

After taking integral for both sides of the equation:

$$RC = \frac{6}{7} * t$$

For 3ms delay, positive slope line:

$$RC = \frac{6}{7} * 3 * 10^{-3} = 2.57 * 10^{-3}$$

$$R = 257K\Omega; C = 10nF$$

For 2ms delay, negative slope line:

$$RC = \frac{6}{7} * 2 * 10^{-3} = 1.71 * 10^{-3}$$

$$R = 171K\Omega; C = 10nF$$

As in comparator part, I again make some alterations in order to get immaculate values for 2ms and 3ms delay.

For 3ms delay, using $RC = 2.57 * 10^{-3}$, delay turned out to be 3.25ms. Using the values R = 90K and C = 26nF, $RC = 2.34 * 10^{-3}$. Then delay turned out to be 3.03ms. Figures below shows the corresponding delay values for both calculated and altered values of R and C.

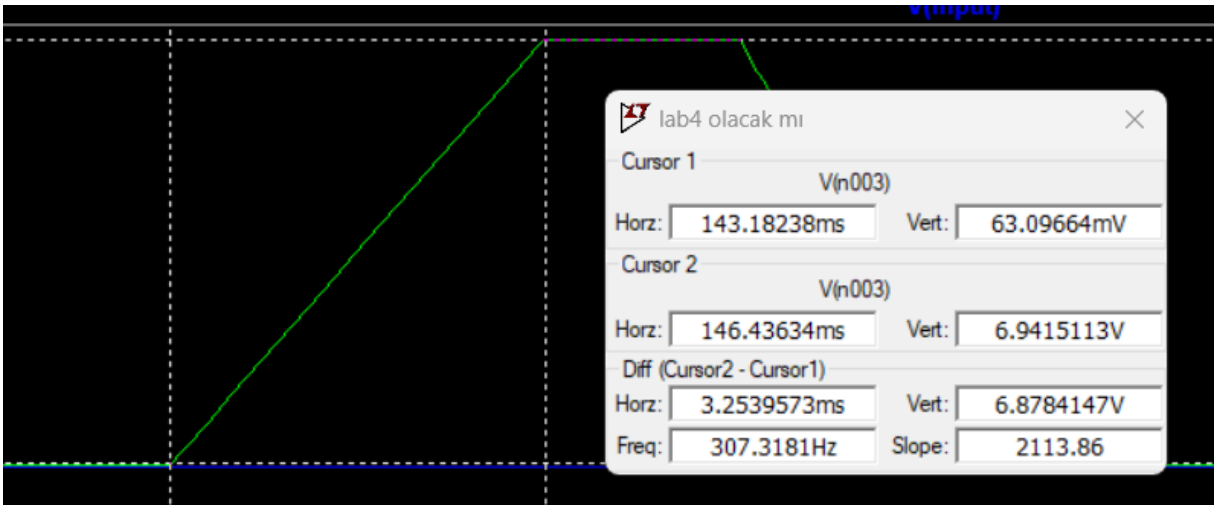

Figure 8: R = 257K; C = 10nF; $RC = 2.57 * 10^{-3}$; delay = 3.25ms

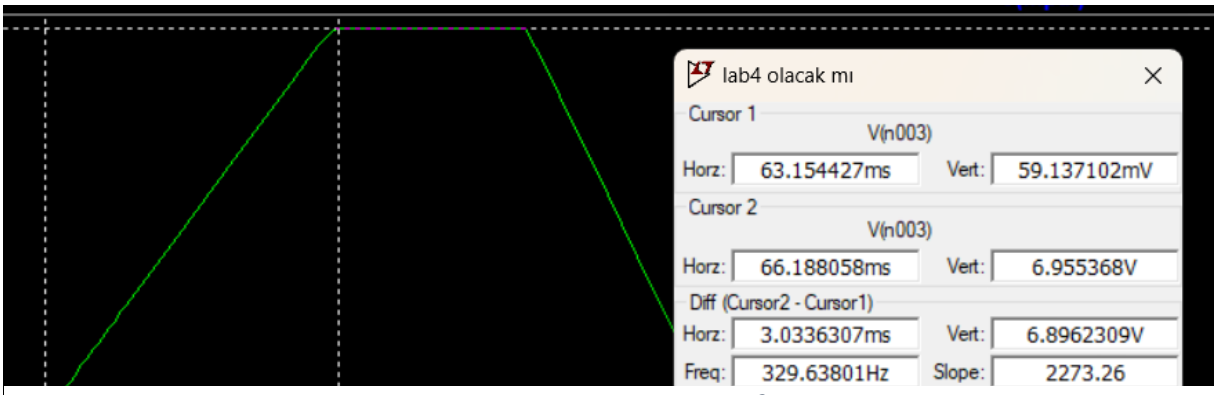

Figure 9: R = 90K; C = 26nF; $RC = 2.34 * 10^{-3}$; delay = 3.03ms

Resistor	Capacitor	RC	Time Delay	Error
257K	10nF	$2.57*10^{-3}$	3.25ms	7.69%
90K	26nF	$1.71*10^{-3}$	3.03ms	1%

Table 3: Error calculation for 3ms delay of integrator 1

For 2ms delay, using R = 170K and C = 10nF, $RC = 1.71 * 10^{-3}$, delay turned out to be 2.03ms. The calculated values are immacualety create 2ms delay, therefore I didn't need to alter the R and C values. Figure below shows the waveform and delay.

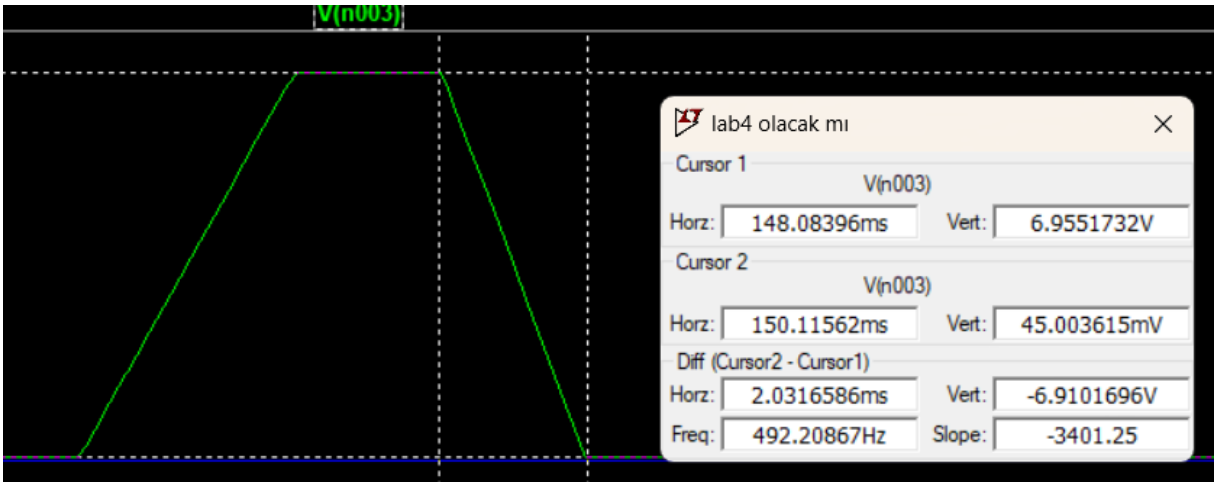

Figure 10: R = 170K; C = 10nF; $RC = 1.71 * 10^{-3}$; delay = 2.03ms

Resistor	Capacitor	RC	Time Delay	Error
170K	10nF	$1.71*10^{-3}$	2.03ms	1.47%

Table 4: Error calculation for 2ms delay of integrator 2

Again, as in the comparator part, looking at (Table 3) and (Table 4), calculated results are lying inside the error bound which is 10% for software implementation.

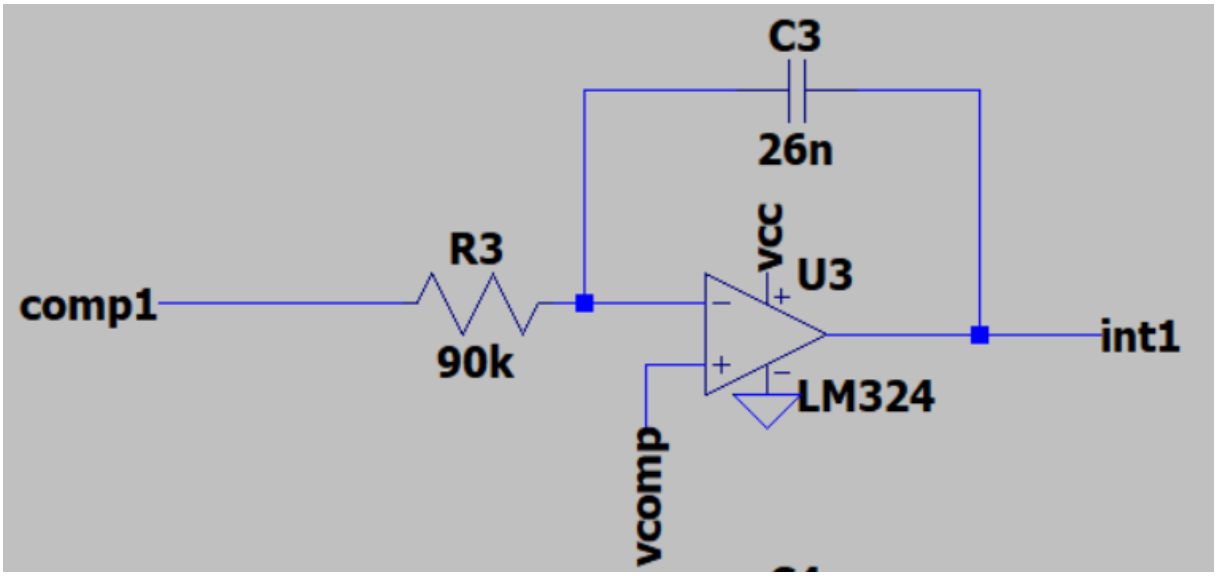

Figure 11: Intergator 1

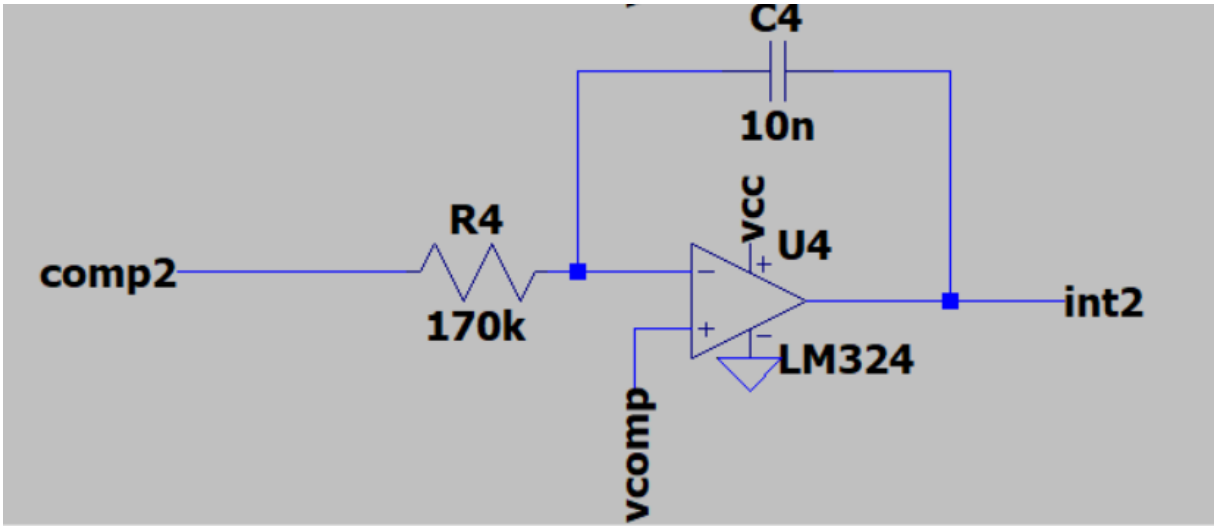

Figure 12: Integrator 2

Subtractor OPAMP

In order to get the final waveform, subtractor OPAMP is used. The principal of subtractor is basically subtracting the inverting and non-inverting inputs of the OPAMP from each other. To obtain the resistor values used in the subtractor OPAMP, KCL is used.

KCL at V-

$$\frac{int1 - V_-}{R8} = \frac{V_- - V_{out}}{R6}$$

After doing some math, V_- is obtained as follows:

$$V_- = \left(\frac{int1}{R8} + \frac{V_{out}}{R6}\right) \times \frac{1}{(\frac{1}{R8} + \frac{1}{R6})}$$

KCL at V_+

$$\frac{int2 - V_+}{R7} = \frac{V_+}{R5}$$

Again aftre some math, V_+ is obtained as follows:

$$V_+ = \frac{int2}{R7 \times (\frac{1}{R7} + \frac{1}{R5})}$$

Using the knowledge $V_+ = V_-$

$$\frac{int2}{R7 \times (\frac{1}{R7} + \frac{1}{R5})} = \left(\frac{int1}{R8} + \frac{V_{out}}{R6}\right) \times \frac{1}{(\frac{1}{R8} + \frac{1}{R6})}$$

If all of the resistor have the same value, then the following equation can be achieved.

$$int1 - int2 = V_{out}$$

I choose resistor values to be 2.2kΩ.

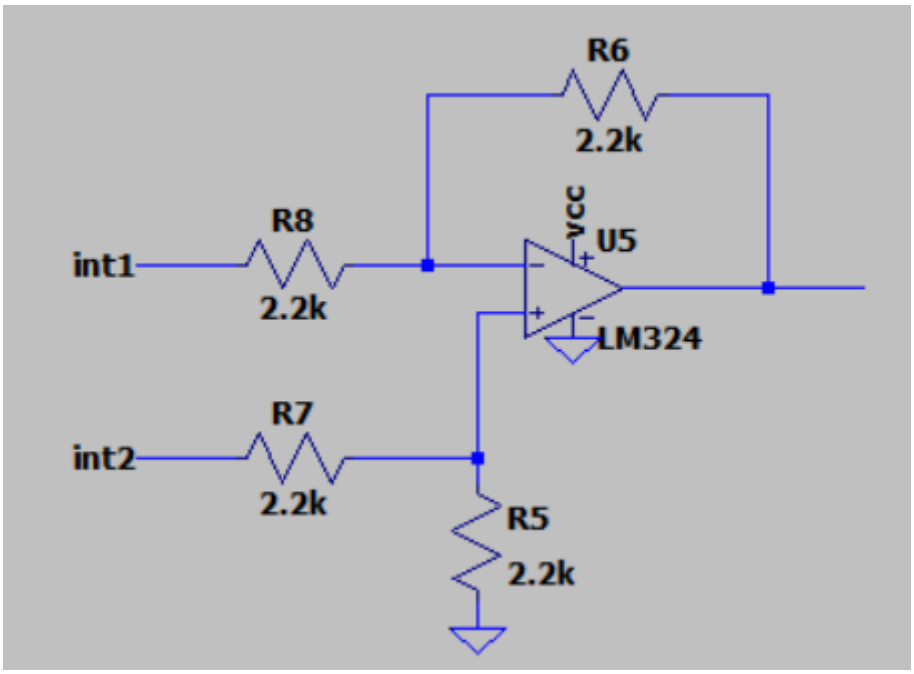

Figure 13: Subtractor OPAMP circuit

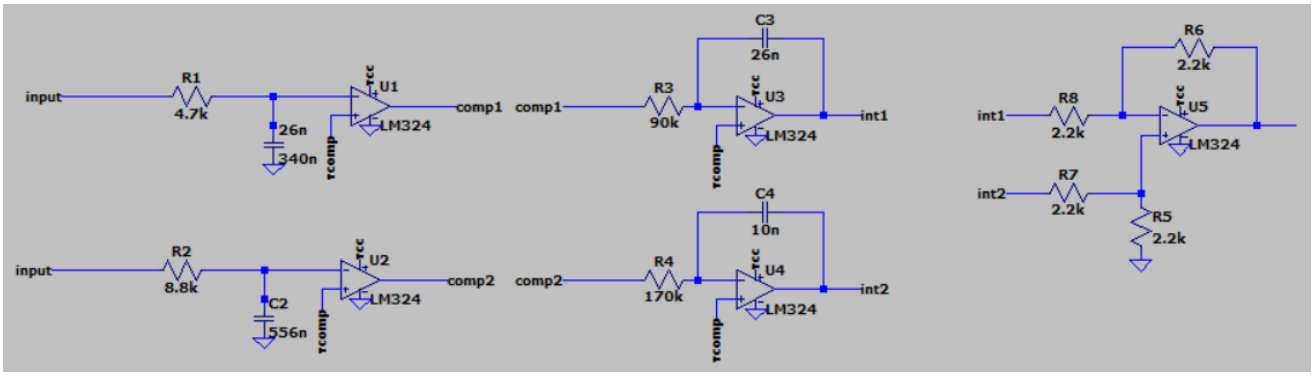

Figure 14: Created circuit

Simulations:

$\Delta t_0 = 3.06ms$ delay can be observed in the figure below.

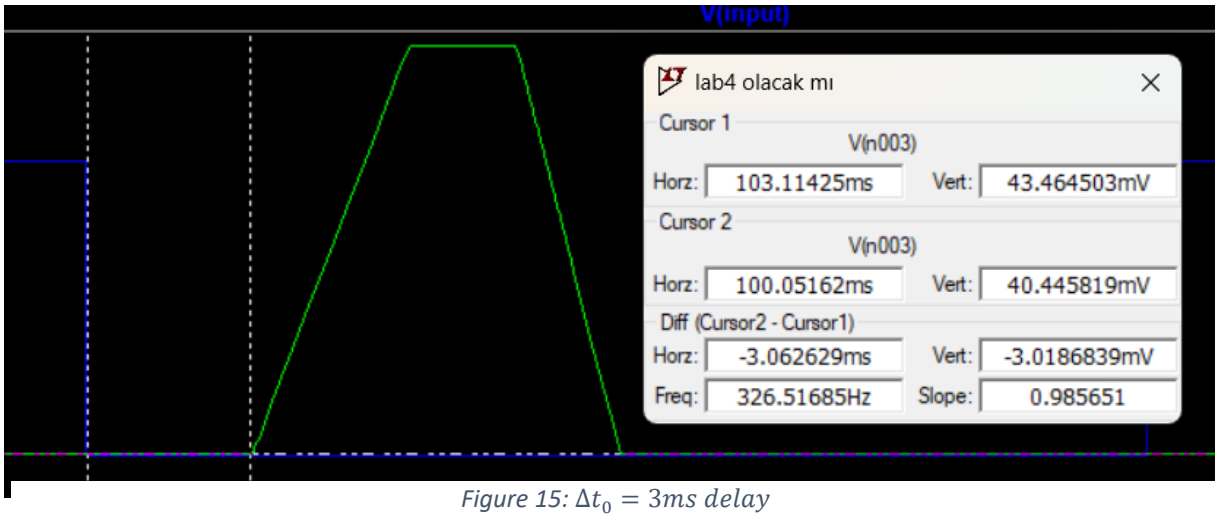

Figure 15: $\Delta t_0 = 3ms$ delay

$\Delta t_1 = 3.02ms$ delay can be observed in the figure below.

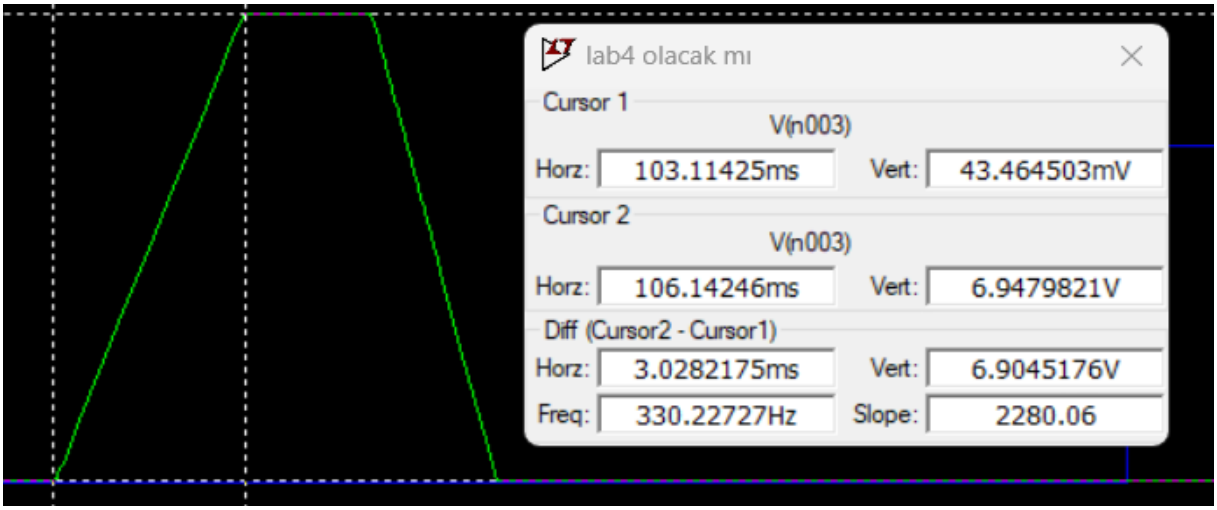

Figure 16: $\Delta t_1 = 3ms$ delay

$\Delta t_2 = 1.96ms$ delay can be observed in the figure below.

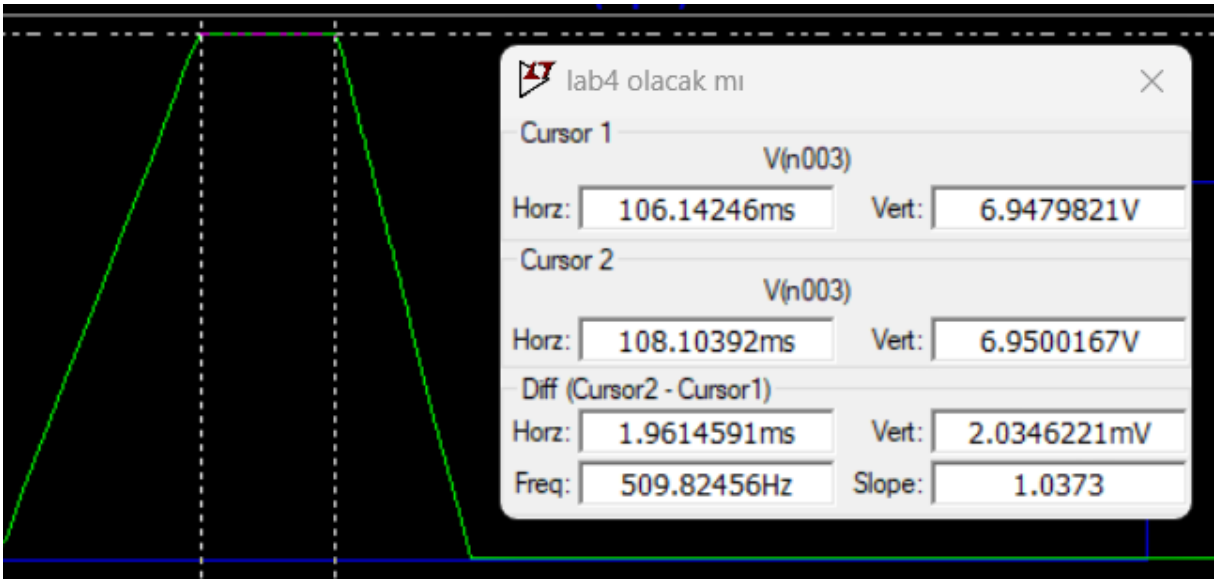

Figure 17: $\Delta t_2 = 2ms$ delay

$\Delta t_3 = 2.03ms$ delay can be observed in the figure below.

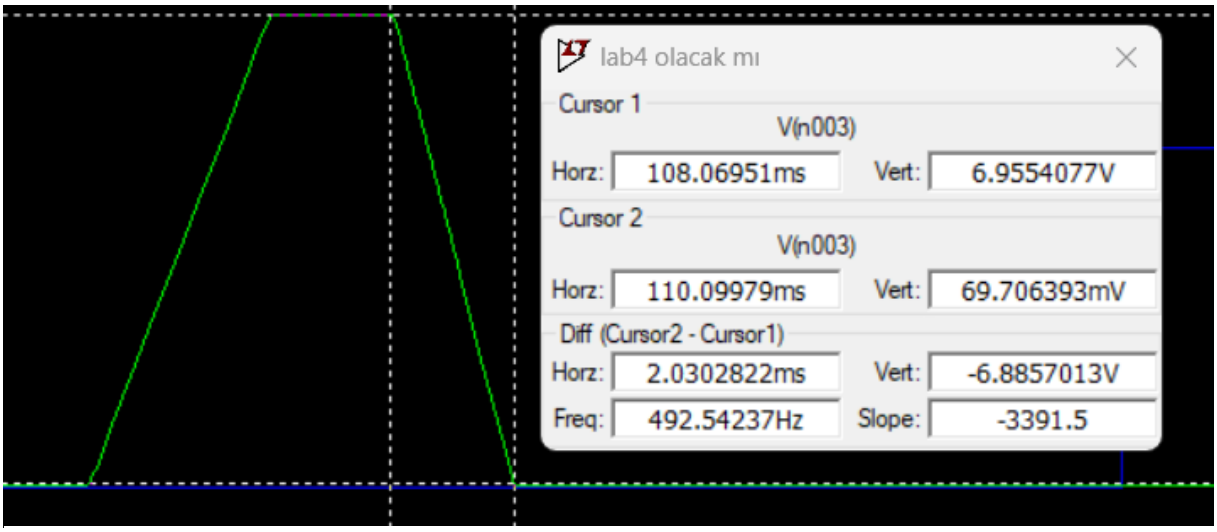

Figure 18: $\Delta t_3 = 2ms$ delay

Also, as seen in (Figure 17), the maximum voltage is 6.95V, which is close to 7V with slight error.

Hardware Implementation:

The hardware design of the desired circuit can be observed in the figure below.

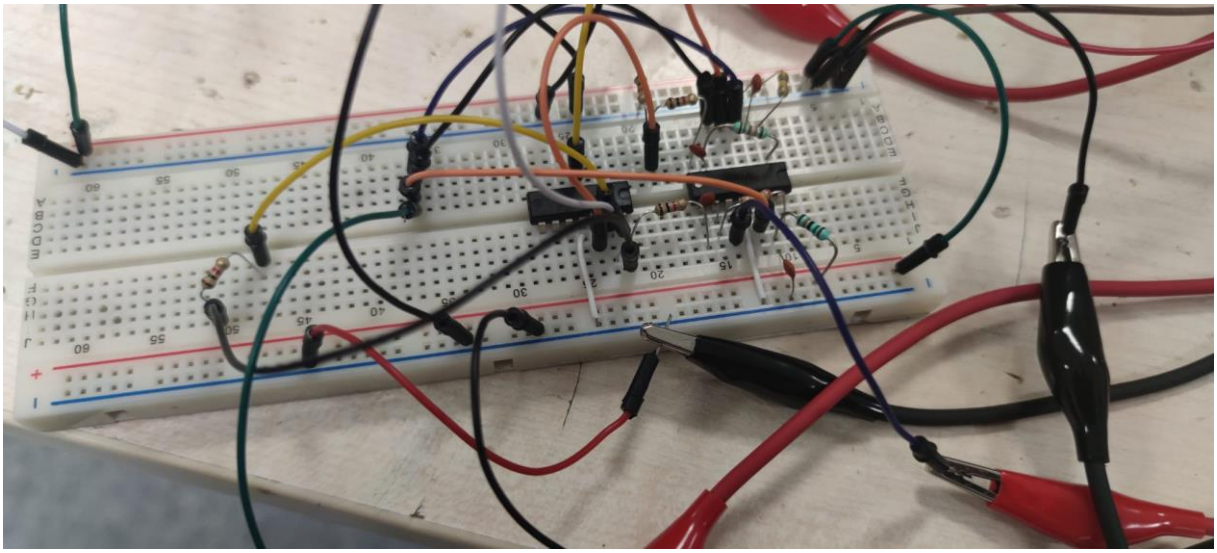

Figure 18: Designed circuit for hardware implementation

To design the circuit, I used two ICs, because one IC only contains 4 OPAMPs. In my circuit, I have 5 OPAMPs. 2 comparator OPAMPs, 2 integrator OPAMPs, and 1 subtractor OPAMP is used.

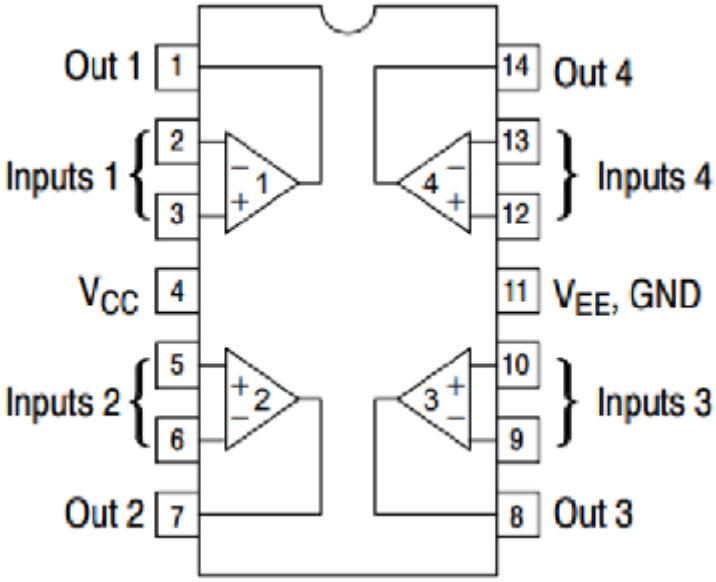

Figure 19: LM-324 OPAMP schematic

The figures below wil show the measured time delays for the hardware implementation of the circuit with 5V, 25Hz square wave input voltage and 8.5V DC as VCC for LM-324. Also, 1V DC input is supplied to all comparator and integrator OPAMP's non-inverting input.

Δt_0 can be seen in the figure below.

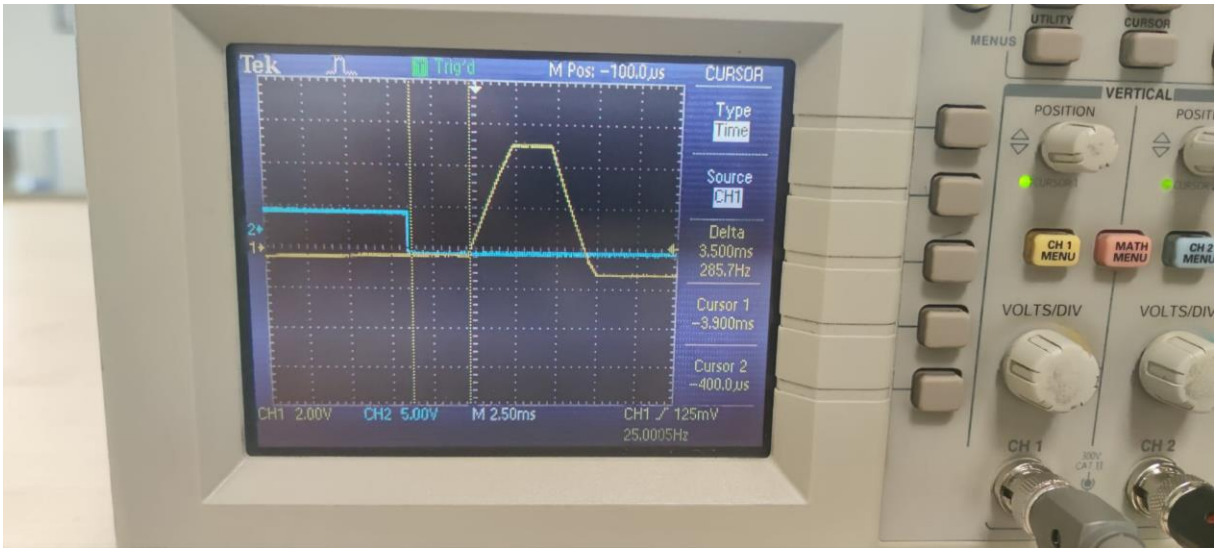

Figure 20: $\Delta t_0 = 3.5\ ms\ delay$

Δt_1 can be seen in the figure below.

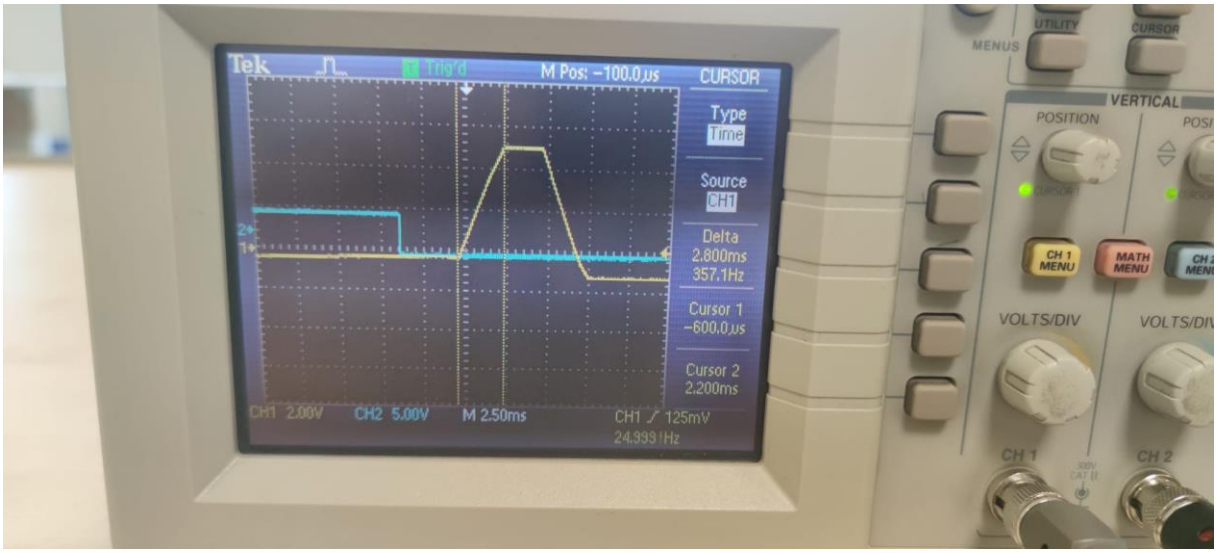

Figure 21: $\Delta t_1 = 2.8\ ms\ delay$

Δt_2 can be seen in the figure below.

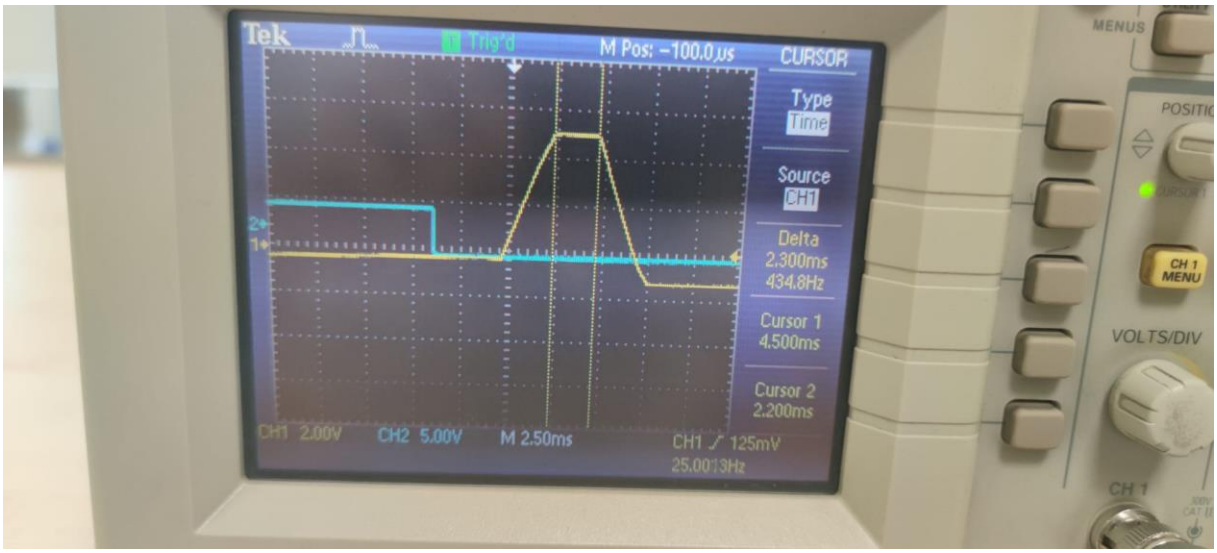

Figure 22: $\Delta t_2 = 2.3\ ms\ delay$

Δt_3 can be seen in the figure below.

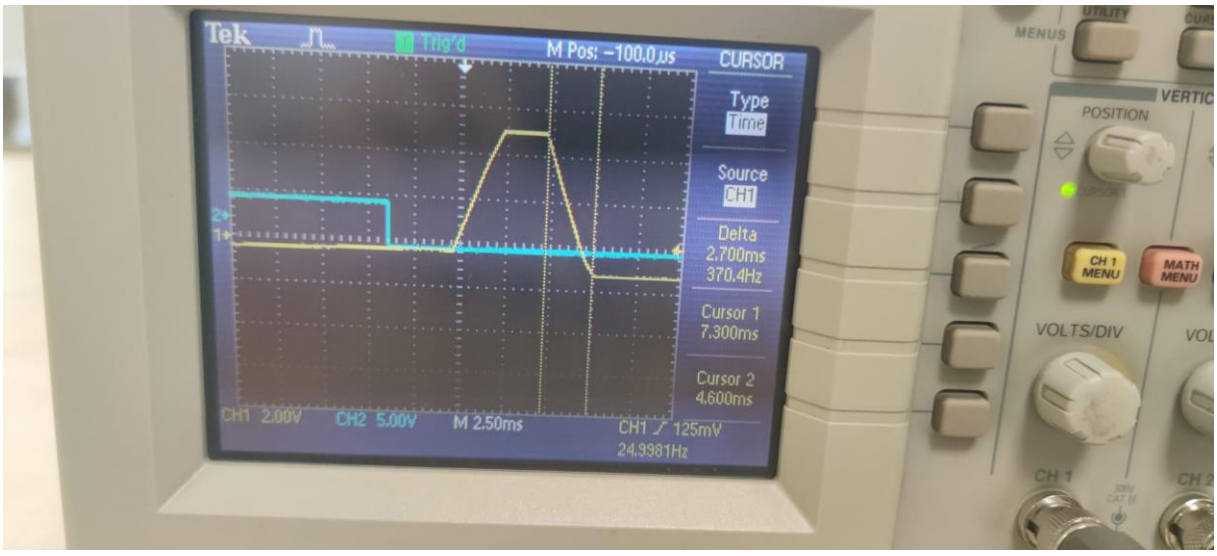

Figure 23: $\Delta t_3 = 2.7\ ms\ delay$

	Δt_0	Δt_1	Δt_2	Δt_3
Hardware values	3.5ms	2.8ms	2.3ms	2.7ms
Error	14.29%	7.14%	13.04%	25.93%

Table 5: Error caclualtion for hardware results

Observing the table above (Table 5), measured time delay values Δt_0, Δt_1, and Δt_2 are lying inside the error bound for hardware implementation which is 20%. However, Δt_3 is exceeded the error limit and turned out to be 2.7ms whereas, it has to be approximately 2ms.

	Δt_0	Δt_1	Δt_2	Δt_3
Software Values	3.06ms	3.02ms	1.96ms	2.03ms
Hardware Values	3.5ms	2.8ms	2.3ms	2.7ms

Table 6: Comparison of hardware and software comparison

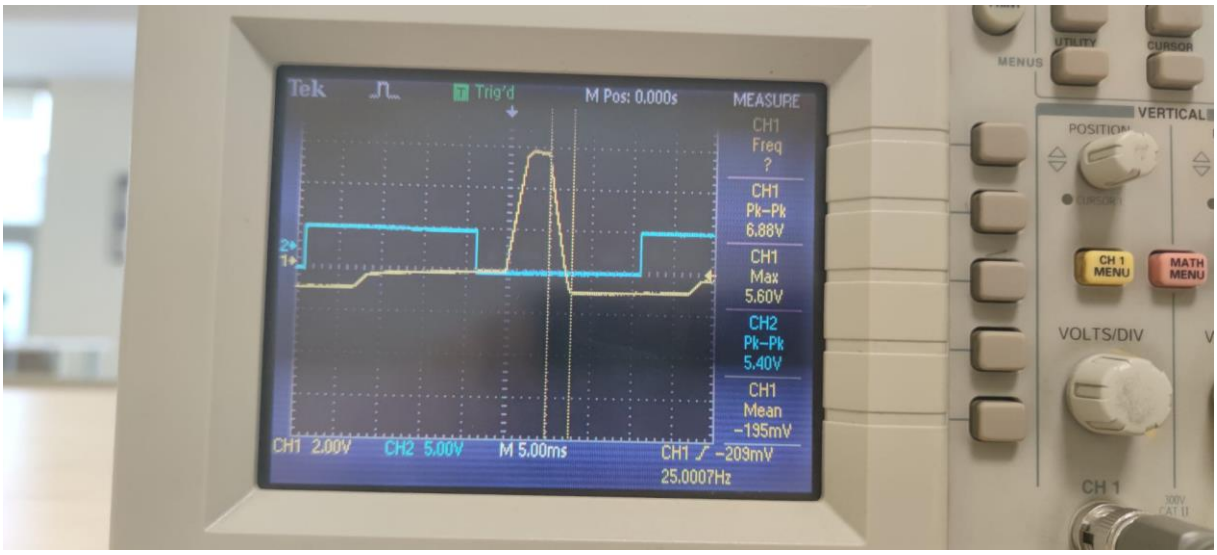

Figure 24: Input and output voltages

As seen in the figure above, output voltage turned out to be 6.88V which is close to 6.95V as found in software implementation with a slight error included.

Conclusion:

The main purpose of this experiment is to design a circuit which generates a trapezoid waveform (Figure 1) using OPAMPs. The maximum voltage circuit can reach is 7V. Input voltage is 5V square wave with 25Hz frequency. To achieve this waveform, 2 comparator OPAMPs, 2integrator OPAMPs, and 1 subtractor OPAMP is used. For software part, due to the experimenter's lack of sensitivity while dragging the cursor at LTspice may resulted in some slight differences of the values obtained. Also, as I mentioned in the software part, I made some alterations on resistor and capacitor values after finding the RC values for corresponding delays. I did these alterations in order to get a more exact time delays as the experiment wants from me. In the hardware part, due to the instability of signal generator, loose contact of the breadboard, insensitivity of the experimenter, and inavailability of desired capacitor and resistor values resulted in some errors and differences in the measurements. All of the measurements except the Δt_3 are resulted in the given error bound for hardware implementation (20%). Error for Δt_3 resulted in 25.92% which is higher than 20%.