Full Name: Orkun Kök

Course Code: EEE202

Section: 02

Experiment Number: 01

Date: 15.10.2023

Lab 1: Time-Domain and Frequency-Domain Analyses in LTSpice

Software Implementation

Introduction (Part 1):

For Part 1, main purpose of the experiment is analyzing the behavior of the output voltage regarding a input voltage. It consists of 2 parts, where in the first part, a voltage divider ciruit is designed and the behavior of the output voltage is viewed. In the second part, an inductor is swapped with one of the resistors and output voltage is analyzed regarding different frequency values given from the input voltage.

Methodology (Part 1.1):

In the first part (Part 1.1), It is asked to create a simple voltage divider circuit in LTSpice and analyze its behavior.

I choose the following voltage and resistor values fort his experiment:

$R_1 = 6\ \Omega$

$R_2 = 12\ \Omega$

V = 6V sinusoidal with 10 kHz

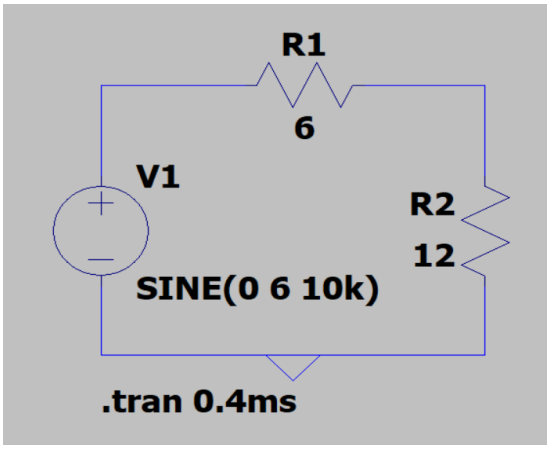

Figure 1.1: Schematic of the first circuit

Analysis:

From the voltage divider formula:

$$V = V1 \times \frac{R2}{R1 + R2}$$

Eq. 1: Voltage Divider Formula

I calculated the voltage on R_2 to be 4V.

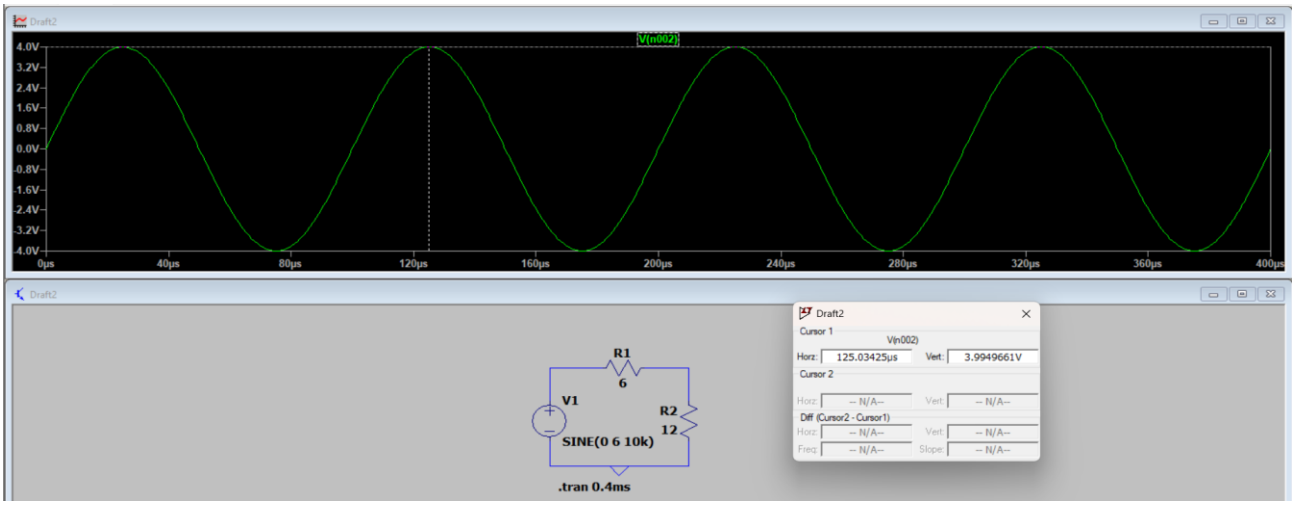

Figure 1.2: Output Voltage at R_2

In the simulation, the result came out to be 3.994 Volts which is very close to 4 Volts.

Calculation	Simulation
V_{Out} = 4 V	V_{Out} = 3.994 V

Table 1: Comparison of calculation and simulation datas for Part 1.1

Methodology (Part 1.2):

In the second step of first part (Part 1.2), it is asked to design a RL circuit by replacing the R_2 in Figure 1.1 with an inductor.

In this step, I choose the following values:

$R_1 = 20\ \Omega$

$L_1 = 10\ \mu H$

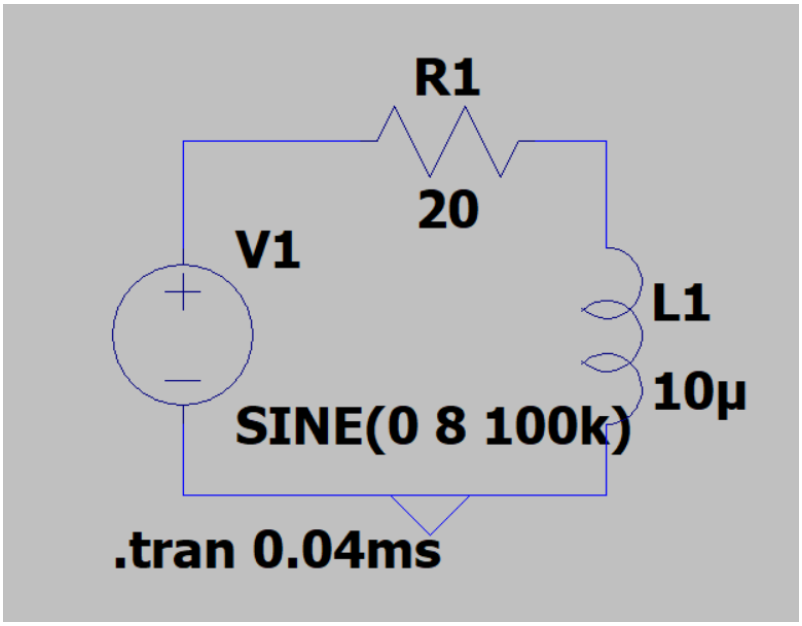

Figure 1.3: RL Circuit that is designed

Simulation:

For 8 V input with 100 kHz, the plot (Figure 1.4) shows that while the input voltage is 8 Volts, the output voltage is only about 2.4 Volts.

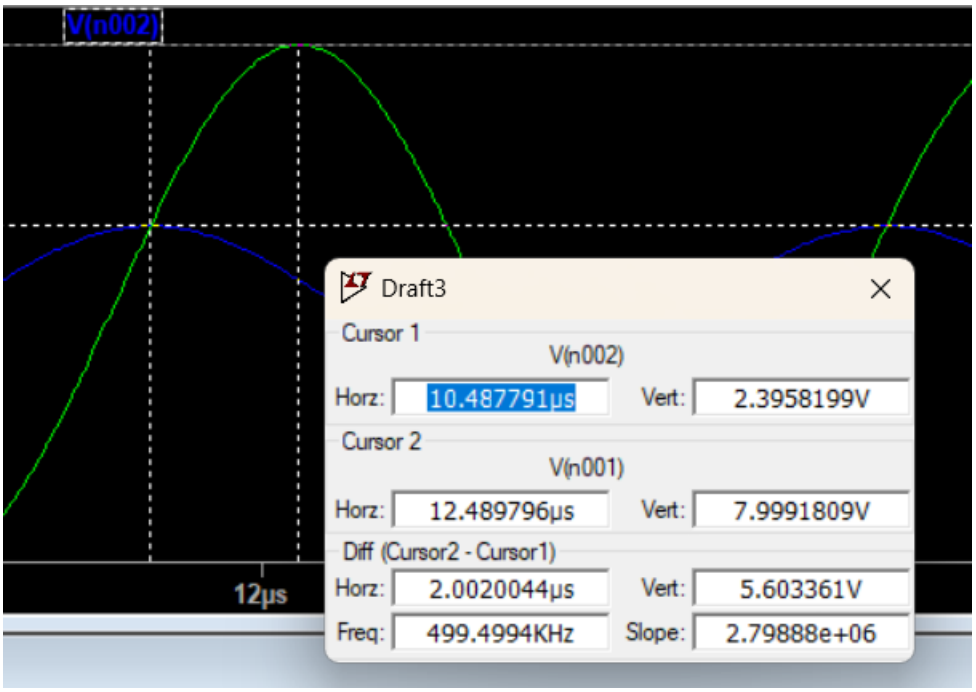

Figure 1.4: Input and Output Voltages for 8 V 100kHz voltage source

For 8 V input with 500 kHz, the plot (Figure 1.5) shows that while the input voltage is 8 Volts, the output voltage is 6.7 Volts.

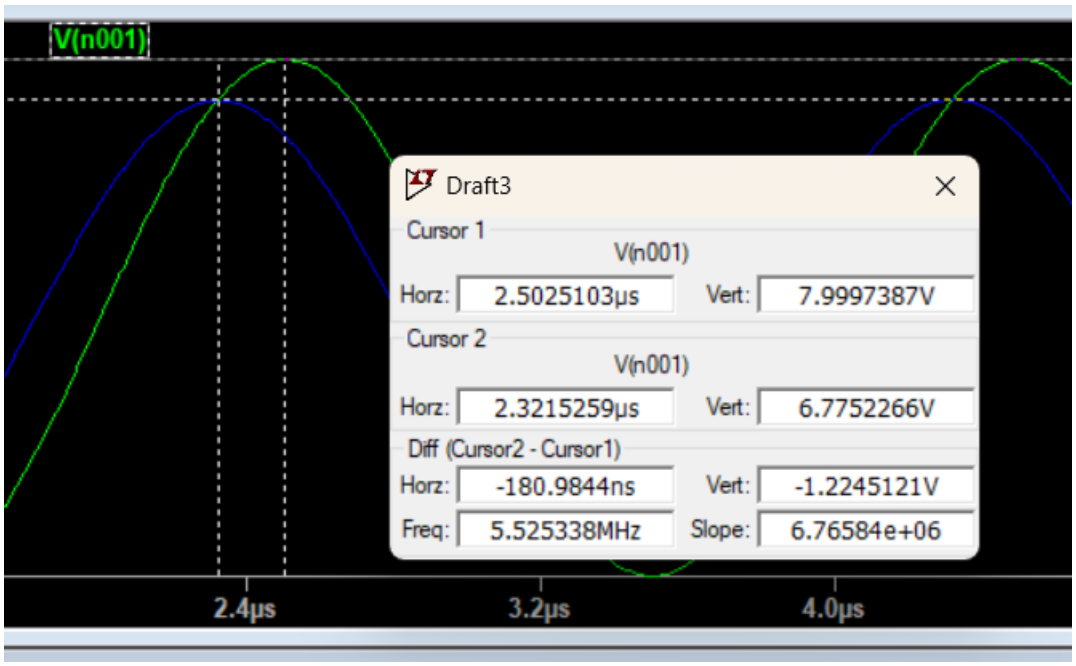

Figure 1.5: Input and Output Voltages for 8 V 500kHz voltage source

For 8 V input with 10 kHz, the plot (Figure 1.6) shows that while the input voltage is 8 Volts, the output voltage is only about 251 mV.

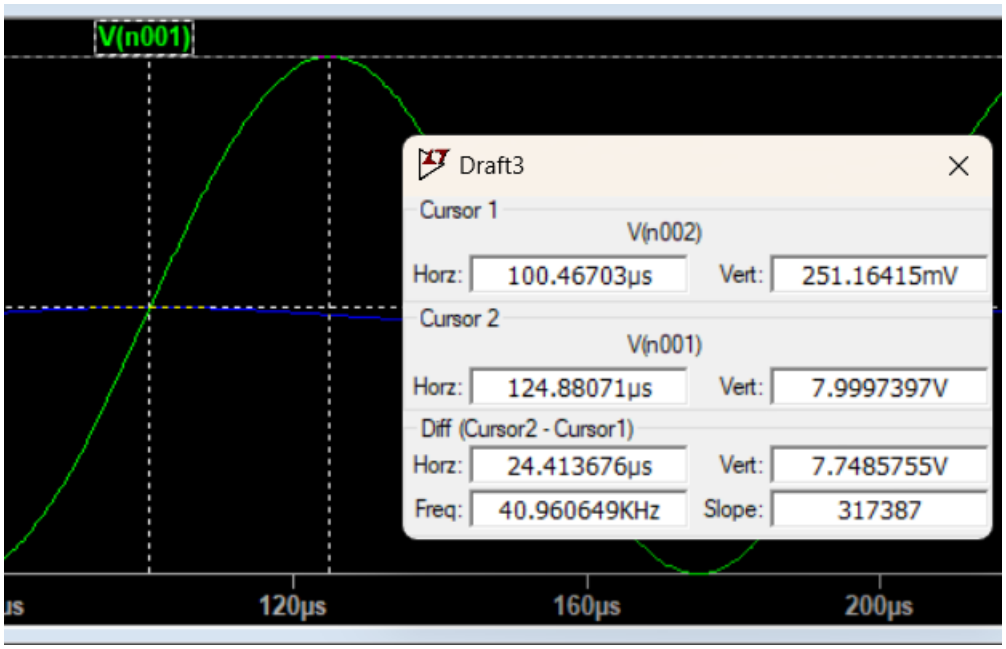

Figure 1.6: Input and Output Voltages for 8 V 10kHz voltage source

V_{in} = 8 Volts 500 kHz	V_{out} = 6.7 Volts
V_{in} = 8 Volts 100 kHz	V_{out} = 2.4 Volts
V_{in} = 8 Volts 10 kHz	V_{out} = 251 mV

Table 2: Input and Output voltages regarding different frequency values for Part1.2

As seen from the results, when the frequency increases, the output voltage also increases, and when the frequency decreases, output voltage also decreases. Therefore, this circuit acts like a high-pass filter.

Methodology (Part 2):

In this part of the experiment, AC (frequency domain) analysis is asked. Main purpose of this part is examining the change in the output voltage regarding the frequency change in a Logarithmic plot because we want to observe the circuits behavior in a long frequncy interval, therefore AC small signal analysis is used.

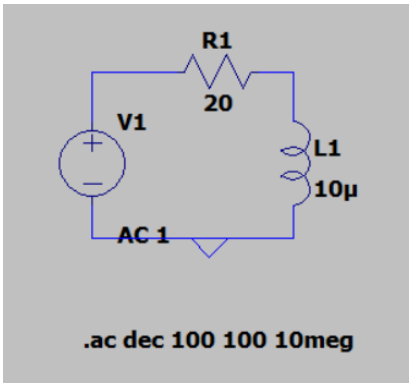

Figure 2.1: RL circuit with small signal AC analysis

Simulation:

The plot of the output voltage at L_1 in decibels can be seen in Figure 2.2.

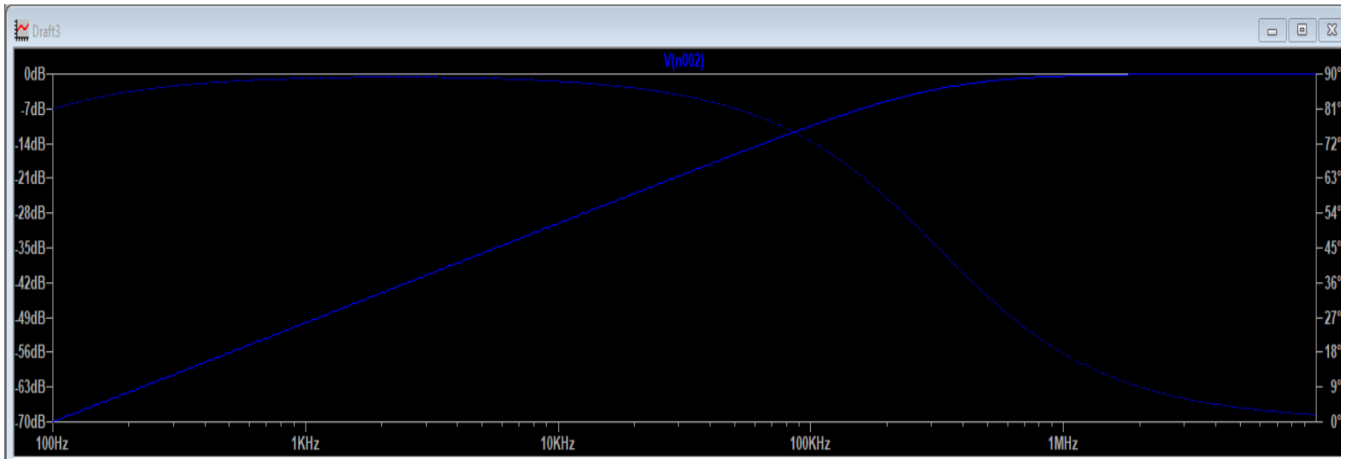

Figure 2.2: Logarithmic plot of output voltage at L_1 of the circuit in Figure 2.1

Using the cursor at the LTSpice, -3dB point (cutoff frequency) is found to be 319 kHz. (Figure 2.2)

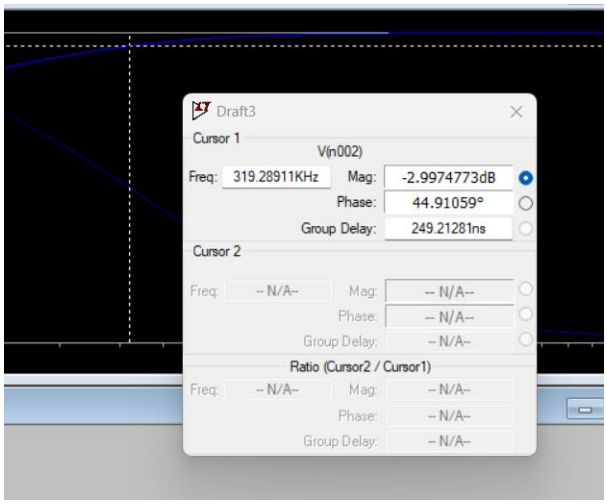

Figure 2.3: -3dB cutoff frequency of
circuit in Figure 2.1

Because signal generators in the lab have a serial output resistance of 50 Ω, I added a 50 Ω serial resistance to R_1.

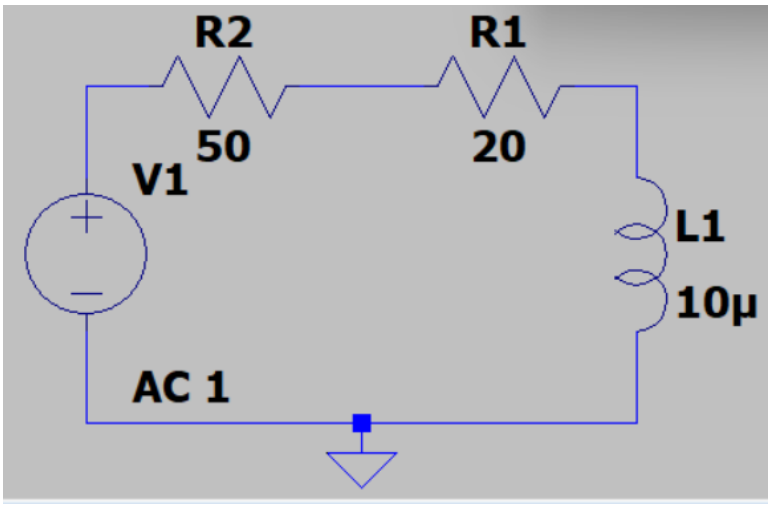

Figure 2.4: circuit in Figure 2.1 with
an extra 50 Ω resistance

The output voltage at L_1 is plotted on dB scale in Figure 2.5.

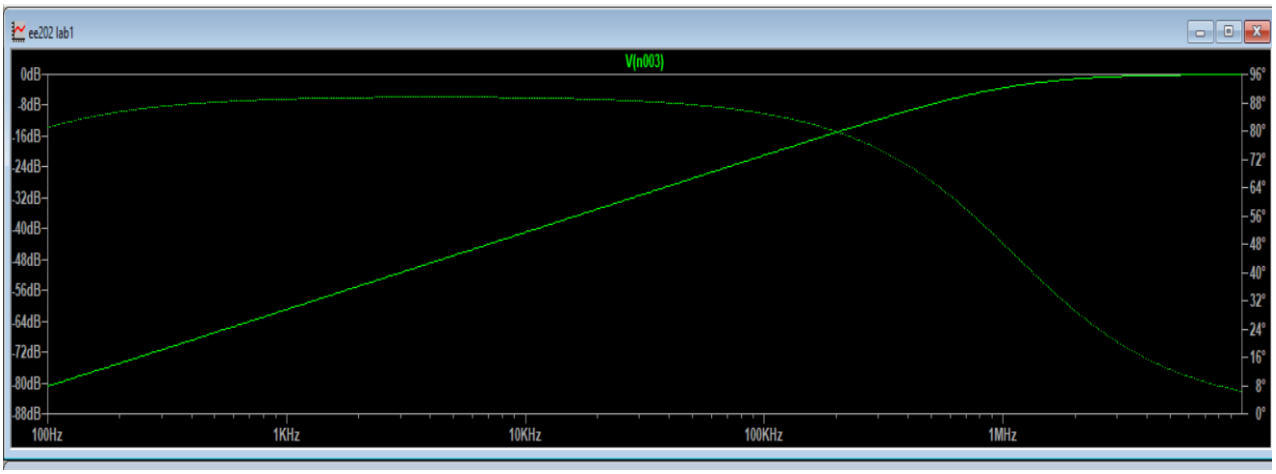

Figure 2.5: Logarithmic plot of output voltage at L_1 of the circuit in Figure 2.4

Again using the cursor at LTSpice, -3dB point (cutoff frequency) is found to be 1.11 MHz. (Figure 2.6)

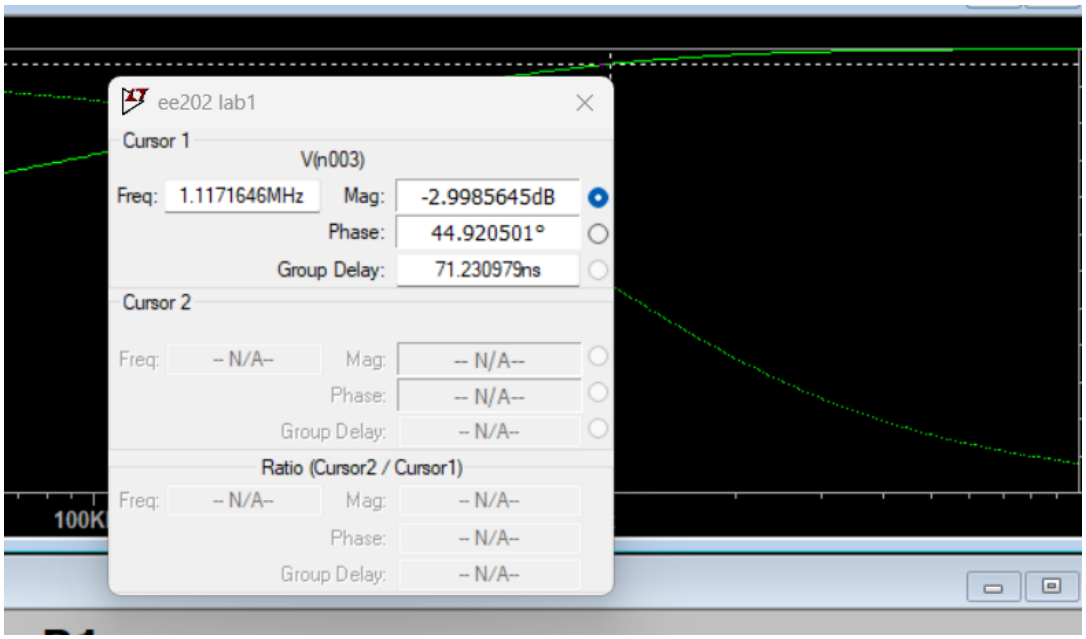

Figure 2.6: -3dB cutoff frequency at the output voltage at L_1 of the circuit in Figure 2.4

Next, I choose the input voltage to be the voltage between 50 Ω and 20 Ω, and plotted the ratio of the output voltage and input voltage. (Figure 2.7)

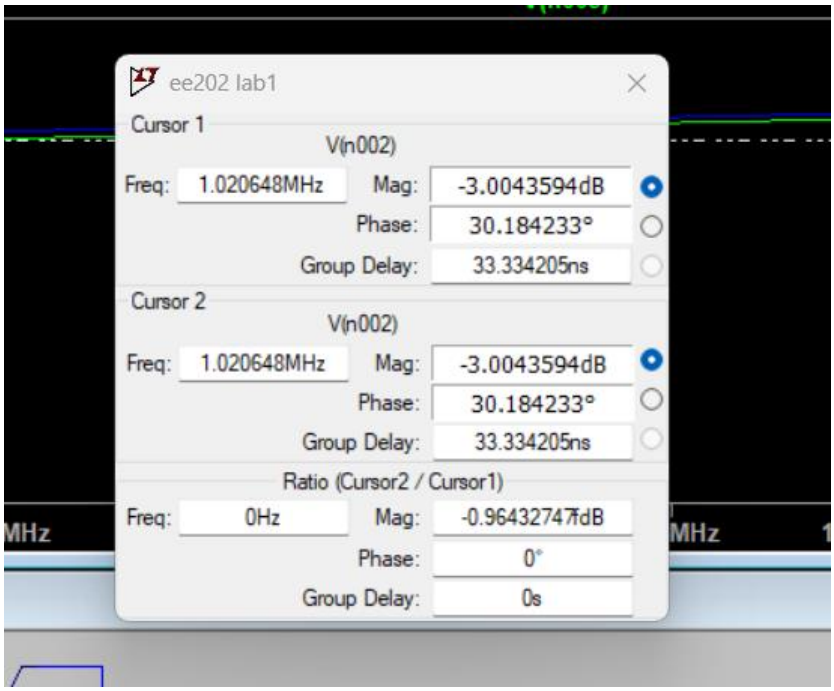

Figure 2.7: ratio of the output at L_1 and input voltage at R_1 and R_2.

Circuit type	V_{in} in dB	-3dB cutoff frequency
No serial resistance, input voltage = AC 1	Input voltage is the same, 0dB	319 kHz
Serial resistance with 50 Ω and input voltage = AC 1	Input voltage not changing, 0dB	1.11 Mhz
Serial resistance with 50 Ω and input voltage different than AC 1 (Voltage between R_1 and R_2)	Input voltage changing, different than 0dB	1.11Mhz however the ratio is equal to 1

Table 3: Cutoff frequencies and Output/Input voltage ratio

Introduction (Part 3):

In this part of the experiment, LM324 OPAMP is wanted to use and given the specific types of circuits, analyze which type of OPAMP circuit is it. The LM324 OPAMP is imported in LTSpice to use it in this experiment. First part of this experiment contaions only resistors and the second part has a capacitor swapped with a resistor in the circuit.

Methodology:

The shown circuit is created with the choosen values of R_1 = 0.5K Ω and R_2 = 1.5K Ω. The DC voltage values that are connected to OPAMP are +8V and -8V. The created circuit can be seen in Figure 3.1.

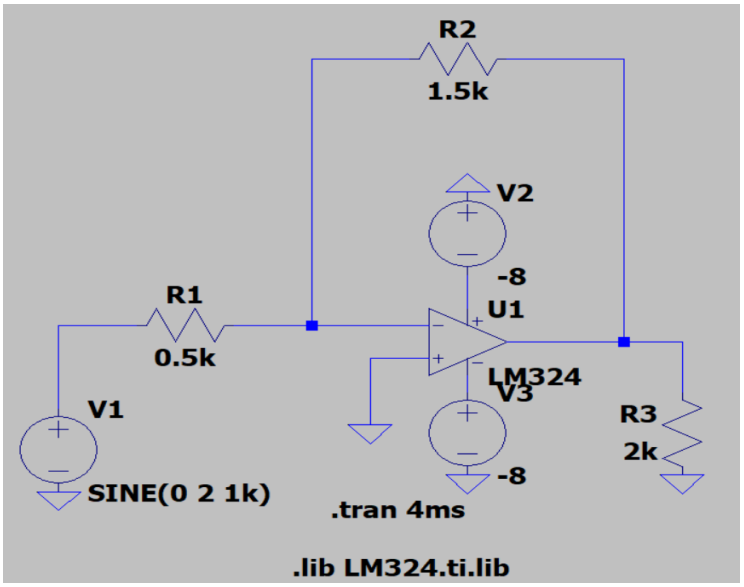

Figure 3.1: Desired OPAMP circuit with the choosen values of R_1, R_2, and V_{cc}.

Simulation:

Looking at the Input (Blue) and Output (Green) voltages on the Figure 3.2, it is seen that the input voltages are both inverted and amplified. This type of an OPAMP is called “Inverting OPAMP”. Input voltage value is 2V and the output voltage value is 6V which can be clearly seen in Figure 3.2.

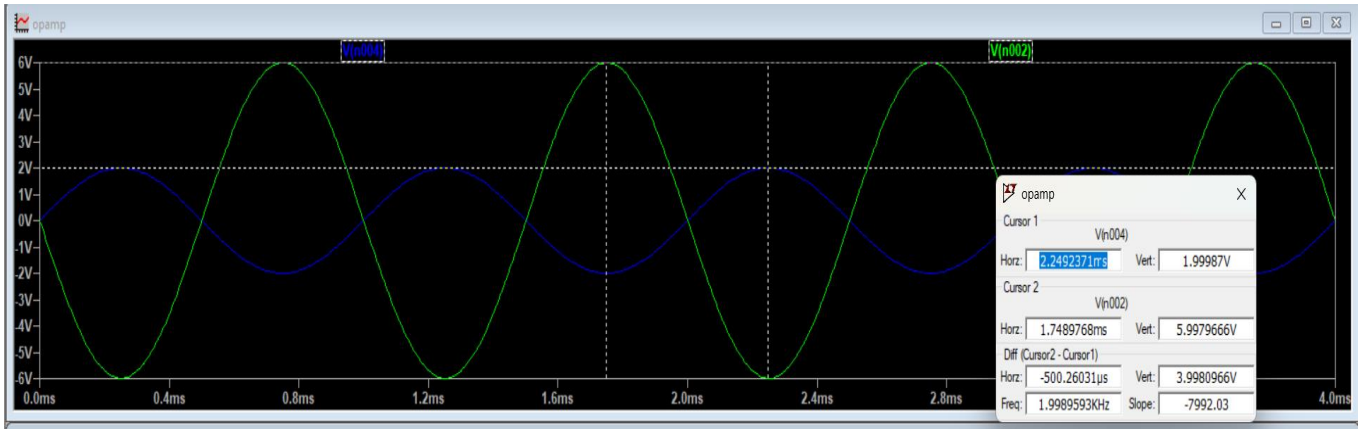

Figure 3.2: Input and Output voltages of the circuit in Figure 3.1

In this step, I changed the sinusoidal voltage wave to square wave. With this change V_{in} = 1V and V_{out} = 3V, with the ratio R2/R1 = 3.

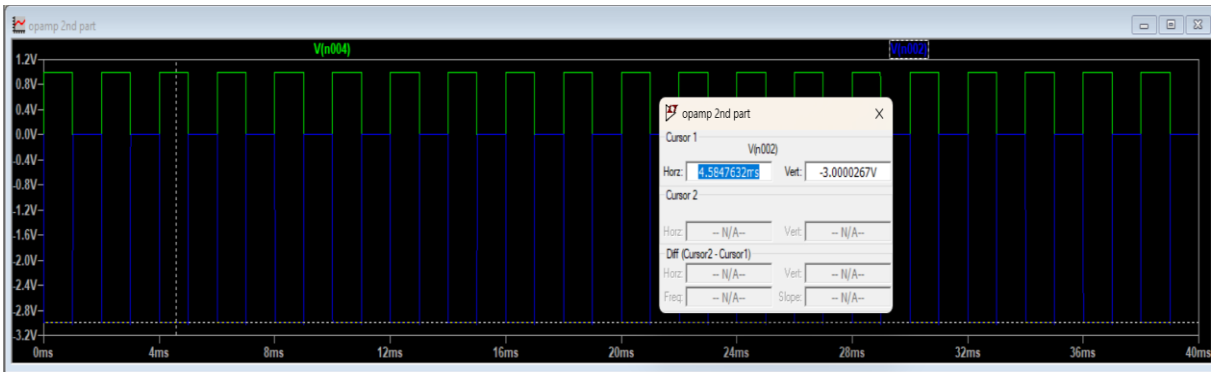

Figure 3.3: R2/R1 = 3, with square wave input voltage, output voltage = 3V

At the beginning of the Part 3, I choose the R_1 and R_2 values as R2/R1 = 3. Now, to find where does the OPAMP reaches its saturation point ($-V_{cc} \leq V_{OUT} \leq V_{cc}$), I increased the R_2 value gradually. At R_2 = 4K Ω, the output voltage reached 7.93 V which is very close to the DC voltage (8V) that I also choose at the beginning. So, at R2/R1 = 8, OPAMP reached saturation point. Figure 3.4 shows the plot of the output voltage at saturation point.

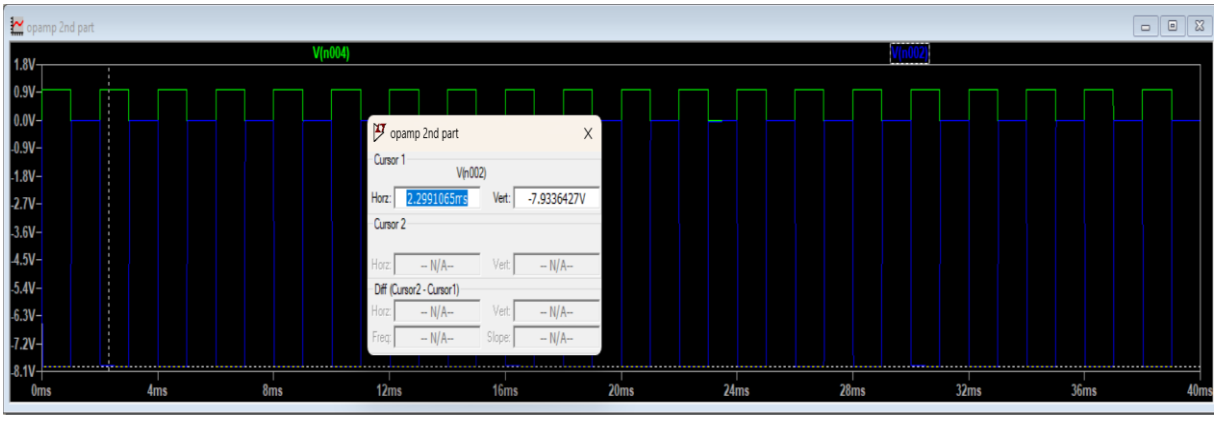

Figure 3.4: R2/R1 = 8, with square wave input voltage, output voltage = 7.93 V

Resistor Ratio	R2/R1 = 3	R2/R1 = 8
Output Voltage	V_{out} = 3V	V_{out} = 7.93V

Table 4: R2/R1 ratio and corresponding output voltage value

For the last part of Part 3, I replace R_2 with a 3nF capacitor and R_1 with 8 K Ω resistor. The new circuit now became a “Integrating OPAMP” circuit. Figure 3.6 shows the behavior of the circuit in Figure 3.5.

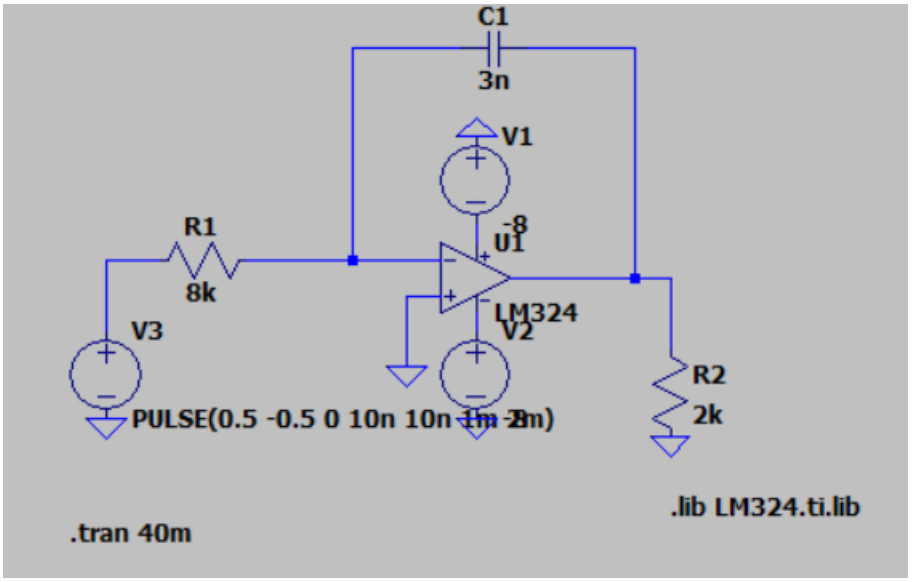

Figure 3.5: New OPAMP circuit with
a capacitor

In order to see both +0.5V and -0.5V in square wave, I changed the initial value 0V to 0.5V and V_{on} from 1V to -0.5V. That way the expected output voltage is obtained with triangular waveforms (Figure 3.6). Also the output voltages min and max voltages are -7.99 V and 6.49 V.

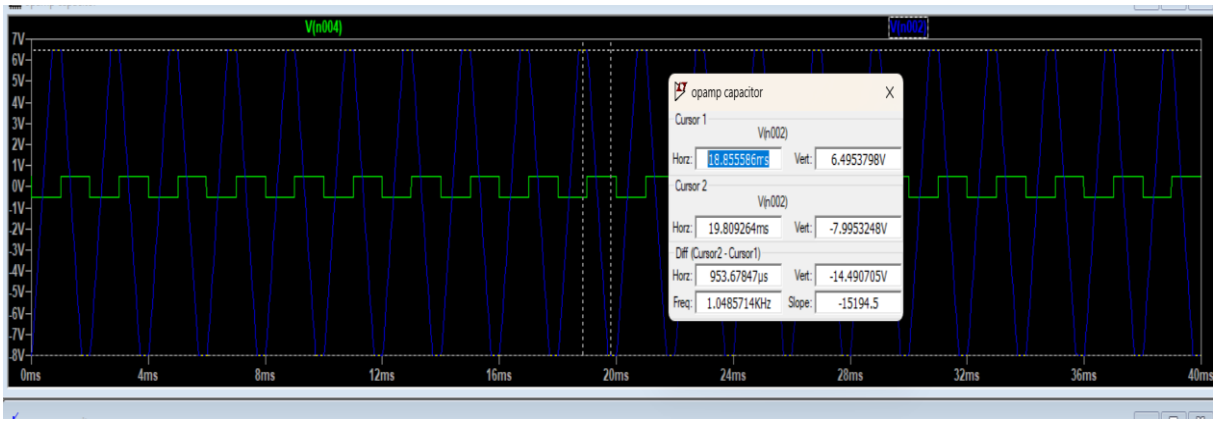

Figure 3.6: Plot of the output voltage
in the circuit Figure 3.5

In the “Integrating OPAMP” circuit, if the input wave is in square waveform, output wave will be triangular due to the intregration.

Hardware Implementation

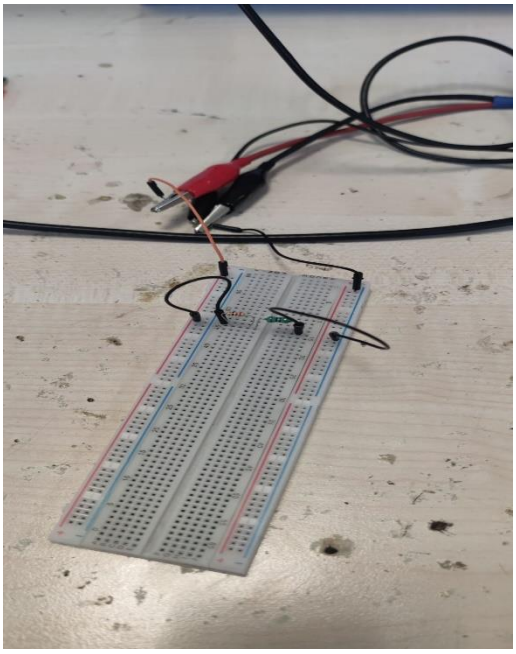

Figure 4.1: RL circuit in Figure 1.3

In software part, I used 20 Ω resistor however, in lab, there is not any 20 Ω resistor available therefore I choose 22 Ω resistor while doing the hardware lab. I used 10µH axial inductor that is available at the lab.

Simulation:

For 8V sinusoidal 100 kHz input voltage, I get 2.22V as output voltage. (Figure 4.2)

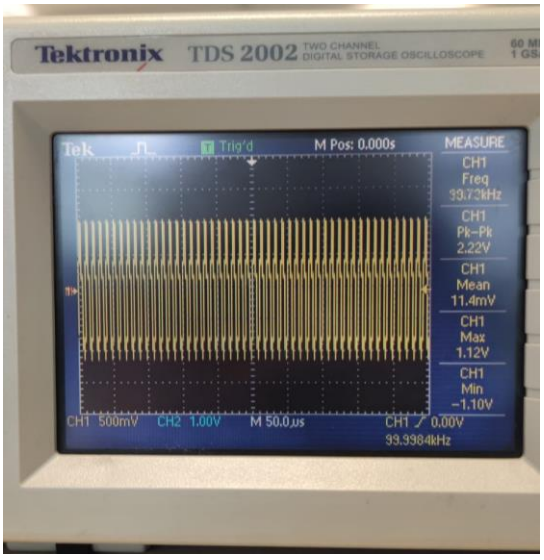

Figure 4.2: RL circuit in Figure 1.3
with frequency 100 kHz, V_{out} = 2.22V

When I changed frequency value from 100kHz to 500kHz, output voltage increased to 5.80 V.

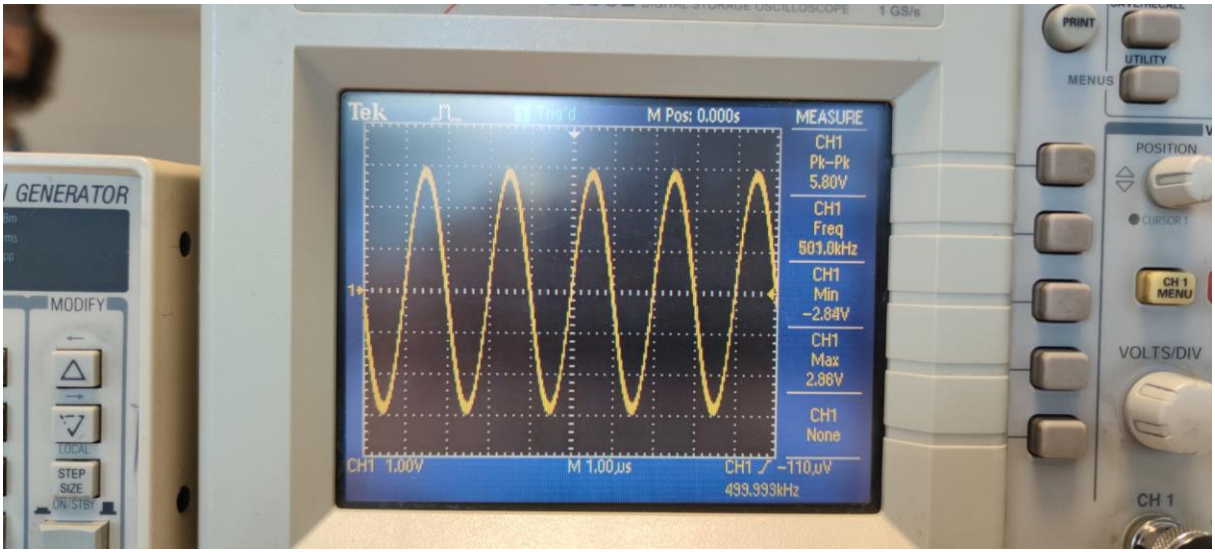

Figure 4.2: RL circuit in Figure 1.3
with frequency 500 kHz, V_{out} = 5.80V

Lastly, when I changed the frequency value to 10kHz, output voltage decreased to 336 mV.

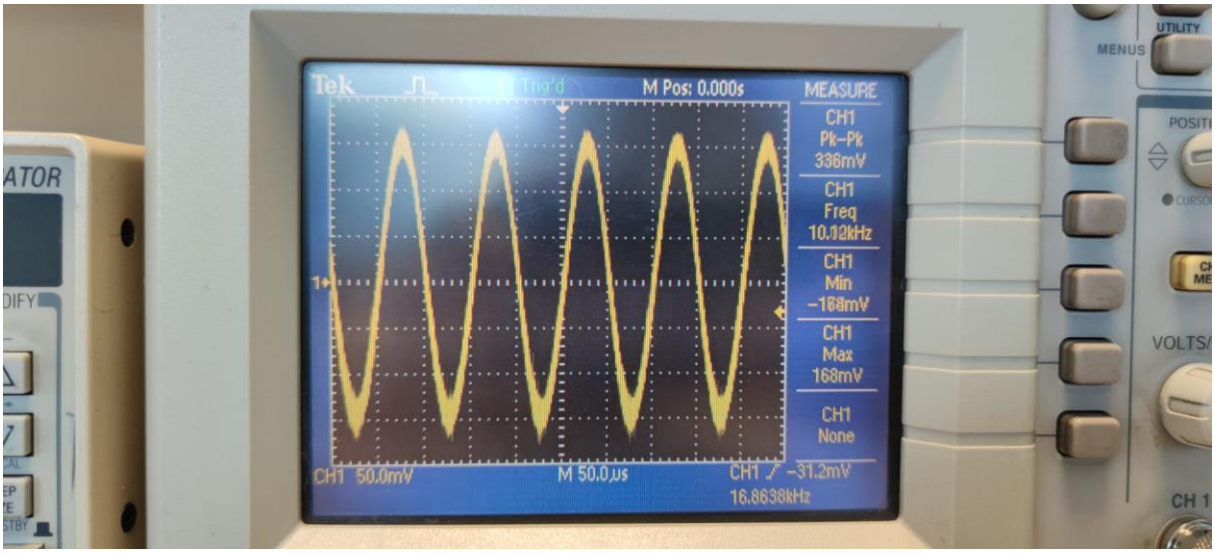

Figure 4.3: RL circuit in Figure 1.3
with frequency 10 kHz, V_{out} = 336 mV

	Hardware lab	Software lab
f = 10kHz	V_{out} = 336 mV	V_{out} = 251 mV
f = 100kHz	V_{out} = 2.22 V	V_{out} = 2.4 V
f = 500kHz	V_{out} = 5.80 V	V_{out} = 6.7 V

Table 5: frequncy and output voltage relation for the designed RL circuit

As seen in the software lab, when frequency increases output voltage is also increasing there this circuit is a high-pass filter.

In this last part of the hardware lab, it is asked to create the OPAMP circuit in Figure 3.1 and the output voltage is observed. I used 470 Ω as R_1 and 1.5K Ω as R_2.

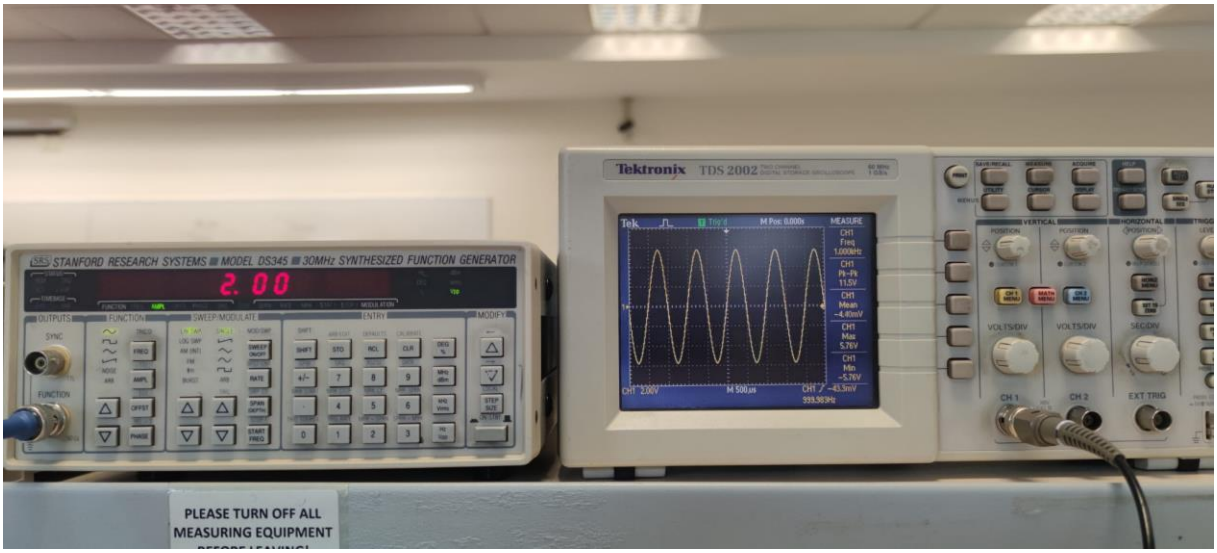

Figure 4.4: Waveform of the output voltage of the OPAMP circuit with V_{in}= 2V 1kHz, output voltage wave, V_{out}max=5.76V and V_{out}min= -5.76V

Software lab	Hardware Lab
V_{out}max = 6V	V_{out}max= 5.76V
V_{out}min = 6V	V_{out}min= -5.76V

Table 6: Output voltages for the OPAMP circuit, comparison of software and hardware lab datas

This circuit is an “Inverting Amplifier” because it amplifies the 2V input voltage to 5.76V output voltage and inverts the input voltage also (e.g V_{in} = 2V and V_{out} = -11.5 V

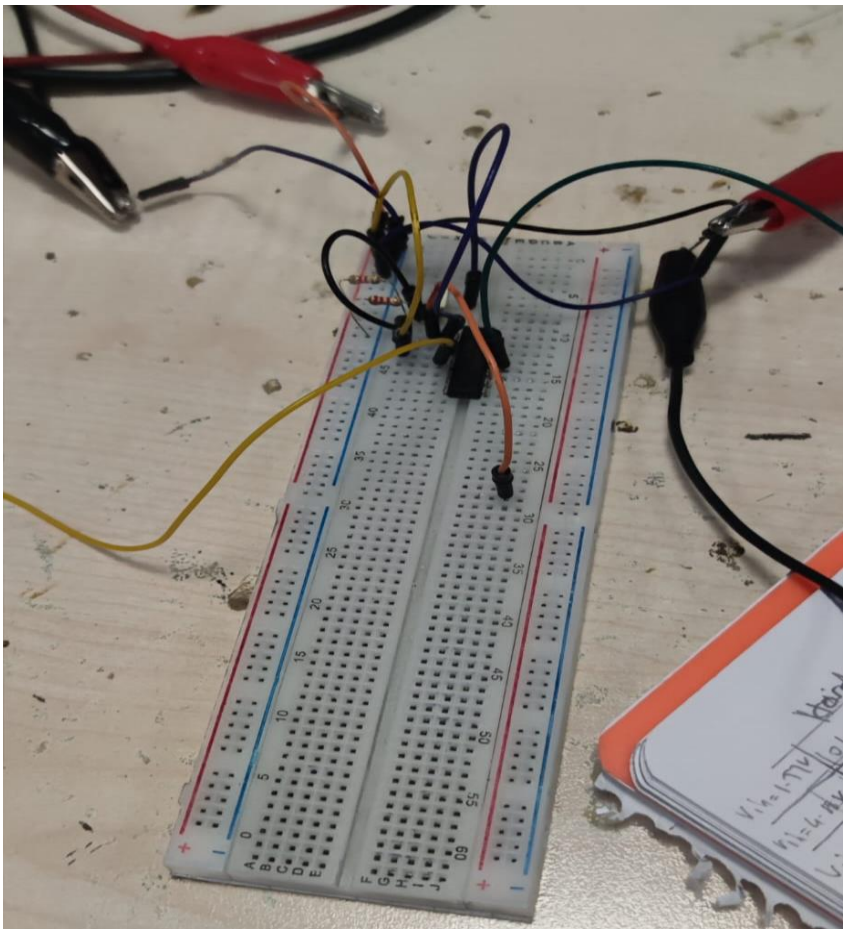

Figure 4.5: Design of the OPAMP
circuit with capacitor

For this circuit, because there is not any 3nF capacitor available, I used 3.3nF capacitor.

Figure 4.6: Output voltage waveform
of OPAMP circuit with capacitor

Software Lab	Hardware Lab
V_{out}max = 6.49 V	V_{out}max= 6.64 V
V_{out}min = -7.99 V	V_{out}min= -7.12 V

Table 7: Output voltages for the OPAMP circuit with capacitor, comparison of software and hardware lab datas

This circuit acts like an “Integrating Amplifier” because we give square wave inputs and the outputs are triangular shaped waveforms. Also, the input voltage is amplified at the output of the OPAMP.

In Part 2 of the experiment, I find the following dB values at LTSpice:

f = 10kHz	-30.86 dB
f = 100kHz	-11.18 dB
f = 500kHz	-1.73 dB
f = 351kHz	-3 dB

Table 8: dB values for different frequencies

Figure 4.7 shows the datas taken from the hardware lab.

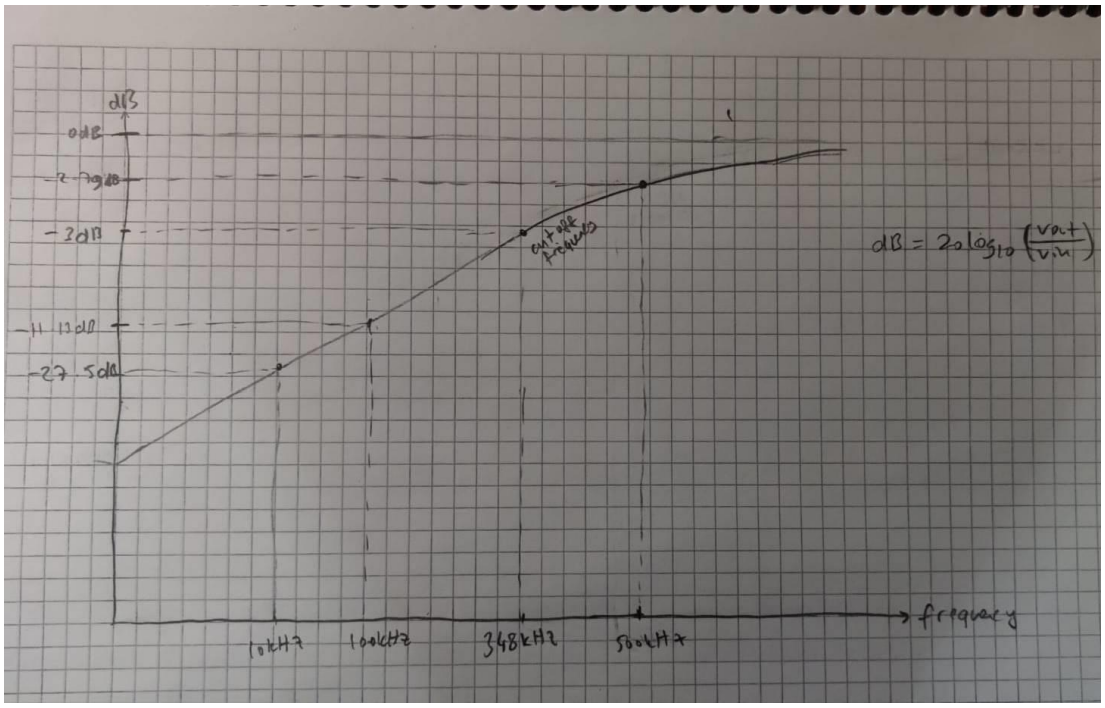

Figure 4.7: dB scale plot for RL circuit

Comparing Table 8 and Figure 4.7, at frequencies 10kHz and 100kHz, datas are very close to each other however, at 500kHz, there is approximateliy 1 dB difference. The difference may occurred due to the experimenter’s insesitiveness or it also may cause from the signal generator in labs.

Conclusion:

The first 2 part of the experiment mainly purposes to examine the time and frequency domain of R and RL circuits. The third part of the assignment relies on the input and output voltage ratios of the OPAMP circuits.

Through experiment, some errors happened. The reason for these errors in hardware labs are caused by the experiment materials, for example in the lab there is not 3nF capacitor and some desired resistor values, therefore experimenter used the nearest values for these materials. Also, some errors caused by the experimenter because it is not sensitive enough while measuring the datas in both software and hardware labs. Nevertheless, there are slight differences between software and hardware lab datas.